Effective implementation methods of FIR filters in FPGA-based signal processing systems

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Abstract **Today's modern FPGA devices and high speed digital to analog converters make it possible to use advanced direct synthesis technologies in semi-professional equipment. However this market segment is usually cost-sensitive, that's why effective usage of available hardware resources is important. This paper analyzes implementation techniques of one of the most resource-consuming building blocks – FIR filters, special attentions is paid to multiplierless approach. Proposed ways of improving existing methods using hardware resources available in the latest-generation FPGAs.**

Keywords **FIR, FPGA, MCM, DUC, direct synthesis.**

I. INTRODUCTION

There are many ways of digital generation of high-frequencies communication signals like DVB-C, DVB-T, LTE, etc. The most commonly used technique is narrow-band (usually 4-16 carriers) generation at lower IF with external analog upconversion, which obviously provide to limited scalability. Newest generation of DACs available on the market with 5-12 giga samples per second make it possible to break the limit and generate full band from the single DAC. For example in CATV applications 96 DVB-C channel can be generated in useful frequency band.

However generating such signal require huge amount of computations for digital upconversion with majority workload needed for FIR filters. Classical ways of implementation of FIR filter use multiplications implemented on hardware multipliers available in any modern FPGA. However multipliers is one of the most limited and power-consuming resource of the FPGA.

That's why in many cases the only way is to use different multiplierless techniques for FIR filters implementation. In this paper the authors presents analysis of such techniques and show that full-bandwidth DUC for CATV applications can be implemented on mid-scale modern FPGA.

II. PROPOSED SOLUTION

Classical way of implementation FIR filters is either systolic multiply-accumulate or transposed multiply-accumulate structures [1] using multiplications. These structures are very efficient in case where time multiplexing can be utilized, i.e. signal sampling rate is lower than system clock. However in described applications signal sampling rate is often much higher than system clock and polyphase filters are used. This mean that number of multiplications needed equals to number of unique filter coefficients (6-20 for typical filters) multiplied by numbers of phases (typically 8) – and even single FIR may use all available hardware multipliers.

However in [5] authors show that FIR can be transformed to mathematically identical structure with separate multiplier block. Implementation of MCM block is analyzed in many works [4], [5] and many algorithm has been suggested, e.g. MAG, RAG, OFL.

Analysis of these algorithm let us make a conclusion that mathematically-optimal solutions often are not implementation-optimal taking into account FPGA resources and limitation. We can state that OFL algorithm is optimal for FPGA implementation.

Besides MCM problem which is deeply analyzed, another field of interest is addition. Modern FPGA logic resources allow to implement very efficient ternary adders and adder trees [3]. With assumption that FIR filter has positive or negative symmetry this can give further reduction of required workload.

We believe that application of ternary adders to MAG graphs can gives yet another possibility of workload reduction, however computational complexity of this problem doesn't allow us provide results and make this subject of further work.

III. RESULTS AND CONCLUSION

In this paper we analyzed different techniques for implementing FIR filters without multiplications. Resource and power usage estimations has been performed for the selected techniques. Working prototype of digital upconverter for CATV application has been implemented in hardware and outperform any similar solution available on the market in terms of price/quality.

Further investigations and improvements directions has been shown.

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