Control of Three Phase 7-Level CHB Voltage-Source Active Rectifier

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***Abstract* – This paper introduces control algorithm of three-phase seven level cascaded H-bridge operates as voltage source active rectifier. The proposed control strategy combines PI and PR controllers with mathematical model of converter current loop and provide direct current control with voltage balancing. The theoretical conclusions are verified by simulations made for small-scale laboratory prototype.**

Keywords-multilevel converter; active rectifier; current control; voltage balancing

I. INTRODUCTION

This project has been made in cooperation with our industrial partner and the main objective of this research has been the analysis and design of control algorithm for three-phase seven level cascaded H-bridge (CHB) voltage-source active rectifier, connected directly to ac grid without transformer. This multilevel voltage-source active rectifier (VSAR), connected directly to 6kV ac-grid must provide: (i) the sum of dc-link voltage in each phase is equal to demanded value (U_{cw}), (ii) the distribution of dc-link voltage on each power cell is identical to demanded value ($U_{c\_mXw} = U_{cw}/3$), and (iii) Low current ripple and sinusoidal waveform. These three requirements must be ensured by selecting suitable control algorithm.

The solution presented in this contribution is based on CHB converter – this configuration is well-known for medium-voltage CHB converters, e.g. [1]-[11], where it is used as a solution for PV systems connected directly to the power grid, static compensators and active filters, medium-voltage converters for EV charging stations.

The popular modulation technique is in this case phase shifted PWM (PS-PWM), which is well described in many publications, see e.g. [2], [3] and [12]- [14]. The designed converter topology include proposed control algorithm was tested on simulation model for low-voltage converter prototype power circuit diagram shown in Figure 1.

II. CONVERTER CONTROL

Proposed control strategy of CHB VSAR uses three separate control loops (these control loops are the same and each is intended for single phase – a, b, c). These control loops uses PI controller for sum dc-link voltage control (R_{Uc}), PR controller for direct control of the fundamental harmonic of ac current (R_i) and extra voltage balancing PI controllers ($R_{\Delta Uc\_m2}$ and $R_{\Delta Uc\_m3}$). The designed control configuration of CHB VSAR is depicted in Figure 2. . It is standard control strategy providing direct current control for single-phase system (presented e.g. in [15] and [16]) and voltage balancing at individual power cells is adjusted by PI controllers $R_{\Delta Uc_m2}$and $R_{\Delta Uc\_m3}$. These controllers only modify the value of modulation signals (duty cycle) u_{v_m2} u_{v_m3}. Therefore, the voltage balancing is in master mode for first cell (U_{c_m1}) and slave modes for second cell (U_{c_m2}) and third cell (U_{c_m3}).

The control strategy for the phase_a is shown in Figure 2. The PI controller (R_{Uc_a}) is used for control sum of dc-link voltage (ΔU_{c_a}) to required value U_{cw}. This value (ΔU_{c_a} is sum of voltage on separated dc-links of phase_a. It is evident from (1). The output signal of controller R_{Uc_a} is magnitude (I_m) of required current for phase_a. From magnitude I_m and ac source voltage position (ϑ_a) is calculated value of required current i_{wa}, (2). The input value for current controller R_{ia} (proportional resonant controller …PR type) is control error e_{i_a} and it is difference between actual current i_a and required current i_{wa}. The output signal of controller R_{ia} is correction part $u_{v\_PR\_a}$ and this part is summed with the estimate signal $u_{v\_estim\_a}$. The resulting value $u_{v\_m1\_a}$ enters into PWM modulator and by firing pulses is switched the first cell (1xHb) of phase_a. Computation of the estimated signal $u_{v\_estim\_a}$ is based on a simplified model of VSAR and it is necessary to know the magnitude (U_m) and position (ϑ_a) of the ac source voltage (u_a), as shown in the (3). The second and the third cell (1xHb) of phase_a is switched by PWM modulator (in this case PS-PWM with shifted carriers) by using control signals $u_{v\_m2\_a}$ and $u_{v\_m3\_a}$. The value of these modulation signals (duty cycles) are adjusted with respect to balancing of dc-links cell for the phase_a. As a balancing controllers are used PI controllers $R_{\Delta Uc\_m2}$ and $R_{\Delta Uc\_m3}$, these controllers only modify the value of modulation signals (duty cycles) $u_{v\_m2\_a}$, $u_{v\_m3\_a}$ against the main signal $u_{v\_m1\_a}$. as a shown in Figure 2. The correction output signals ($\Delta u_{v\_m2\_a}$, $\Delta u_{v\_m3\_a}$) are multiplied by the sign of requirement current magnitude ($sign(I_m)$). The main modulation signals (duty cycles) $u_{v\_m2\_a}$ is calculated from the phase current i_a and sum of dc-links voltage ΣU_{c_a}. The PS-PWM with shifted carriers is used for the modulation of converter. The major benefit of employed shifted carriers is the

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significant decrease of the ac current ripple due to multilevel nature of the voltage at the converter ac terminals. In our particular case with three modules in series, the phase-voltage at the converter ac side is seven-level (Illustration of modulation and saw signal with resulting phase voltage at the converter ac terminals is depicted in Figure 3. The number of voltage levels for CHB converter is given by (4). The shifted carriers and resulting reduced ac current ripple have positive impact on the converter input inductance design (There is less transitions between voltage levels – 7 levels).

$$\sum U_{c\_a} = U_{c\_m1\_a} + U_{c\_m2\_a} + U_{c\_m3\_a} \quad (1)$$

$$i_{wa} = I_m.sin(\vartheta_a) \quad (2)$$

$$u_{v\_estim\_a} = U_m.sin(\vartheta_a) \quad (3)$$

$$V_{levels} = 2.N + 1 \quad (4)$$

III. Converter Simulation Results

The proposed control of VSAR was tested on simulation model of three-phase CHB converter. This simulation model is composed of three-phase voltage sources (u_a, u_b, u_c), input inductance L, three H-bridge for each phase connected in series. The converter load is simulated by nine individual current sources ($i_{z\_a\_M1}$ - $i_{z\_c\_M3}$). The simulation model of the CHB VSAR has been designed in language C. For the calculation of differential equations we use Euler difference formula of the first order, the simulation step size is of 0.1µs. In this simulation we have tested discreet control algorithm which is depicted in Figure 2. The sampling period of controllers was 50 µs, this short sampling period of control was chosen as to obtain precisely summation at the control algorithm (especially for calculation of resonant controllers).

The Figure 4. shows simulation result of the CHB active rectifier under steady-state condition. The waveforms i_a, i_b, i_c represents ac phase currents which are harmonic and in phase with ac-grid voltage u_a, u_b, u_c. The output dc-link voltage at individual power cells for step change of load from 0 kW to 9.45 kW is shown in Figure 5. In this case the symmetrical load was simulated by nine equivalent current sources ($i_{z\_a\_M1}$=7A, $i_{z\_a\_M2}$=7A, $i_{z\_a\_M3}$=7A, $i_{z\_b\_M1}$=7A, $i_{z\_b\_M2}$=7A, $i_{z\_b\_M3}$=7A, $i_{z\_c\_M1}$=7A, $i_{z\_c\_M2}$=7A, $i_{z\_c\_M3}$=7A). The ripple of controlled dc-link voltages (at each of individual power cell) has the dominant frequency of double grid voltage frequency. This distortion is coming-out from physical properties of single-phase voltage-source active rectifier type of converter. The Figure 6. shows the response of CHB active rectifier to step change of non-symmetrical load ($i_{z\_a\_M1}$=7A, $i_{z\_a\_M2}$=7.3A, $i_{z\_a\_M3}$=7.6A, $i_{z\_b\_M1}$=5.6A, $i_{z\_b\_M2}$=5A, $i_{z\_b\_M3}$=5.3A, $i_{z\_c\_M1}$=5A, $i_{z\_c\_M2}$=6A, $i_{z\_c\_M3}$=7A). The simulation result shows satisfactory operation of the balancing controllers. In this case the non-symmetrical load is reflected in the differences at ac currents value and by the current ripple differences as a shown in Figure 7.

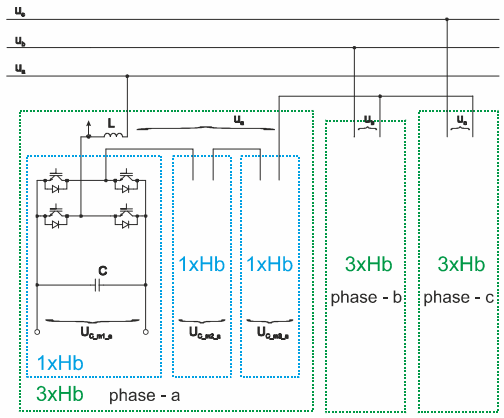

Figure 1. Configuration of designed three phase 7-Level CHB Voltage-Source Active Rectifier

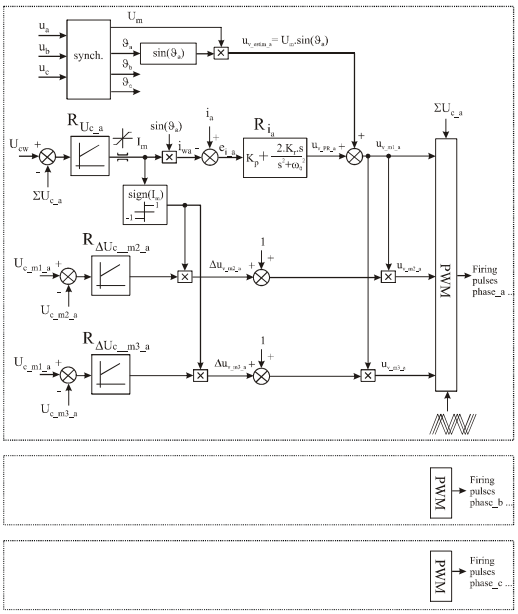

Figure 2. Proposed control of three phase 7-Level CHB Voltage-Source Active Rectifier

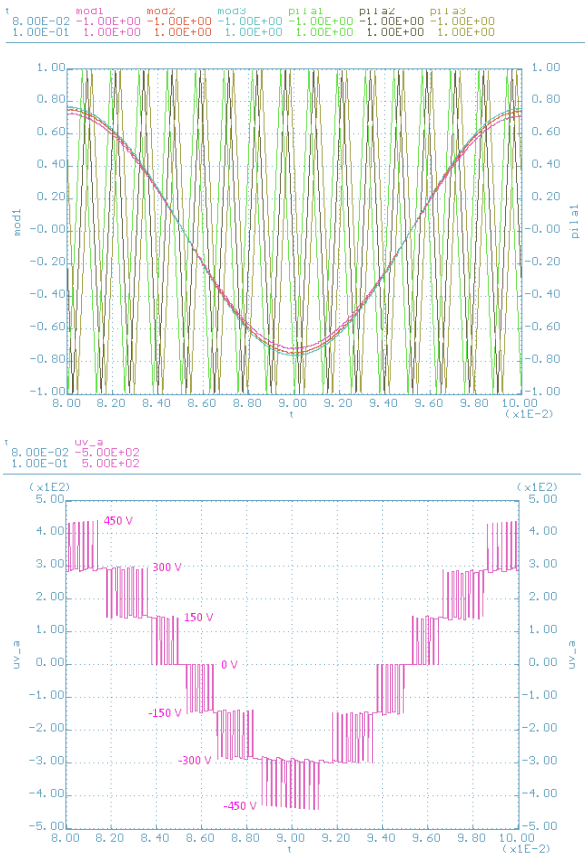

Figure 3. modulation and saw signals with resulting ac voltage phase for single-phase

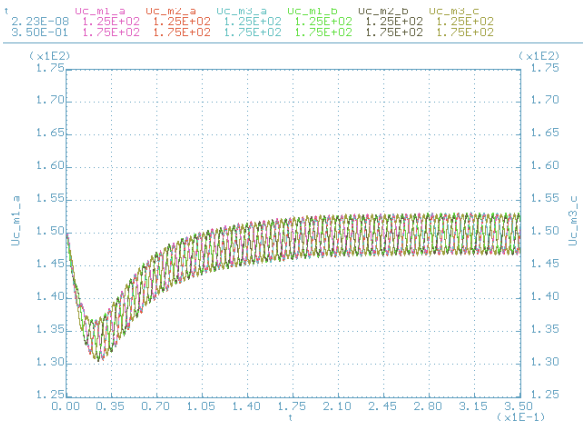

Figure 5. Behaviour of dc-link voltages on selected cells for step change of load (P = 0 kW → 9.45 kW during symmetrical load).

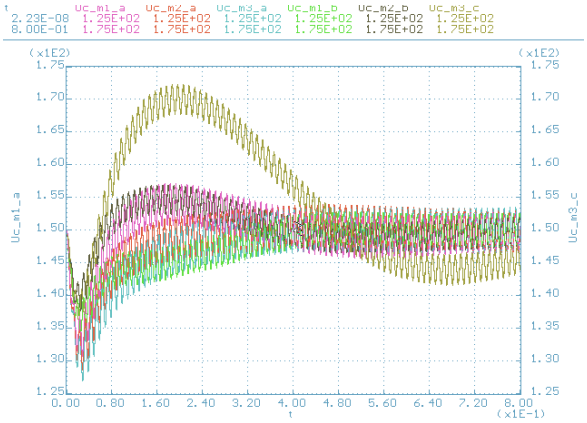

Figure 6. Behaviour of dc-links voltage on selected cells for step change of load (non-symmetrical load).

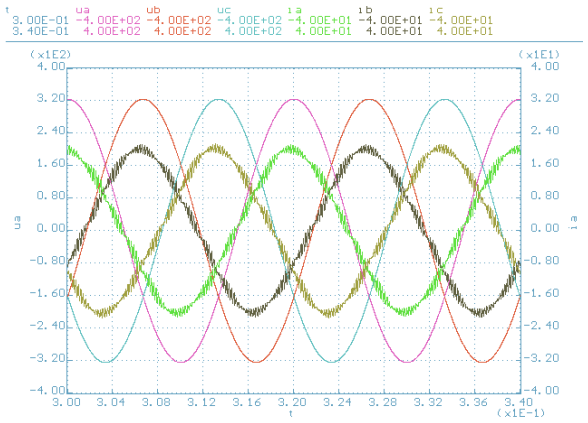

Figure 4. Voltages and currents of VSAR under steady-state conditions in rectifier mode (symetrical load P = 9.45 kW

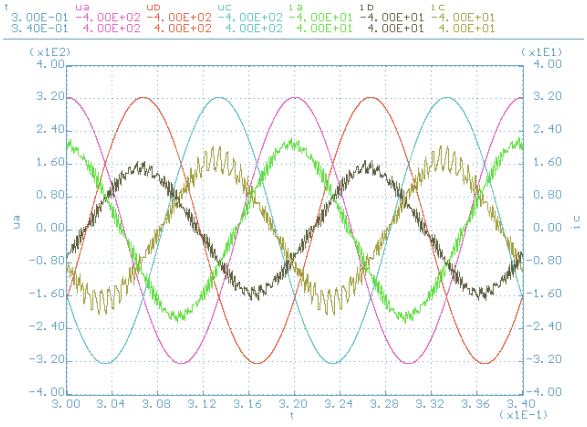

Figure 7. Phase-voltages and currents of VSAR under steady-state conditions in rectifier mode (during non-symetrical load).

IV. CONSLUSIONS

This paper present control designed for cascaded H-bridge voltage-source active rectifier with harmonic current waveform. This control provides a sufficiently fast control of the output dc voltage for step change of the load. Proposed control enables active voltage balancing for each of individual power cells under non-symmetrical converter load (tested for 33% non-symmetrical load of phase c). The control provides voltage balancing on individual power cells directly at the control structure level. This is the simple and powerful approach which can be easily implemented using conventional PR and PI controllers which are industry-standard components. The remaining problems are slow dynamics of balancing one second in this case and voltage balancing during zero load of active rectifier.

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