A Phase Shifted Full Bridge Converter Design for Electrical Vehicle Battery Charge Applications Based on Wide Output Voltage Range

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Abstract – **In this study, high efficiency design procedure of a phase shifted full bridge (PSFB) converter is presented for on-board electrical vehicle (EV) battery charger. Presented design methodology used lithium-ion battery cells because of their high voltage and current rates compared to a lead-acid battery cells. In this case, PSFB converter can be regulated wide range output voltage with while its soft switching operation is maintained. The basic operation principles of PSFB converter is defined and its soft switching operation requirements are given. To evaluate the performance of the converter over wide output voltage range, zero voltage switching (ZVS) operation of converter is discussed based on dead time requirement. To improve efficiency, the snubber inductance effects on soft switching over wide output voltage range are evaluated. Finally, operation of the PSFB converter is validated experimentally with a prototype which has 42-54 V/15 A output range at 200 kHz switching frequency.**

Keywords- Phase shifted full bridge converter, EV battery chargers, high efficiency, wide range output voltage regulation.

I. INTRODUCTION

The use of electrical vehicle (EV) and plug in hybrid EV increases every day due to their advantages in economic area and global warming. The battery charger of EV can be designed on board or off-board. On-board systems provides the flexibility to end user to charge vehicle's battery from any possible power outlet [1]. However, the battery charger brings extra weight, volume and cost to EV as discussed in [2]. The proposed studies in [3] and [4] evaluates the high power density on-board battery chargers. The study in [3] gives the design methodology to reach high efficiency and decreased volume. In [4], integrated on-board chargers are discussed. Integrated chargers use motor windings as filter inductors or transformer and motor inverter is used as bidirectional AC-DC converter so their control and design results in complex solution to implementation.

In order to compete EV with internal combustion engine vehicle, on-board battery charger should be design with high power density, high efficiency and simple structure as discussed in [5] and [6]. Recently, in order to keep power density high, lithium-ion battery cells are usually used because they have higher

voltage and current rate compared to the other battery cell and this provides high power density battery package [7], [8]. In this case, lithium-ion battery chargers can regulate wide output voltage range.

A battery charger usually uses a front-end power factor correction boost converter at the first stage and a dc-dc converter regulates the output voltage at the second stage as designed battery chargers in [9] and [10]. For high power density and high efficiency applications, the soft switching dc-dc converters are usually preferred [2]. The phase shifted full bridge (PSFB) pulse width modulated (PWM) converter [1] and resonant converters [9]-[11] work naturally with soft switching, they don't require additional circuit components. Therefore, they are preferred for the second stage of EV battery chargers. The resonant converter can regulate the output voltage with the change of switching frequency. The frequency change is not desired application in power converter design because the magnetic component optimization is difficult at the changing frequency range. Besides, sinusoidal change of current and voltage values require semiconductors with high rates [12]. PSFB PWM converter works with soft switching by the applying phase delay to control signals of conducted diagonal primary switches. There are a lot of design procedure of PSFB converter for constant output voltage application is presented in the literature [13]-[18]. Among them, [13], [14] and [17] are focused on high efficiency design procedure for data center or telecom applications. The studies, given in [15] and [18], evaluate the light load efficiency improvement with dead time and delay time optimization in server power systems. In [16], an auxiliary circuit is included in PSFB converter to extend soft switching operation range of primary switches for welding machines. The performance of PSFB converter for wide range output voltage regulation, required in li-ion battery chargers, is very different compared to constant output voltage applications mentioned above.

Recently, an on-board battery charger design procedure using PSFB converter is presented in [1] and [19]. In the proposed methods, performance of battery charger is evaluated by the use of SiC power semiconductors. The volume, weight and efficiency of the battery charger is optimized for on-board system. However, the performance and design procedure of

PSFB converter based on wide range output voltage regulation is not discussed in detail.

In this study, a PSFB PWM converter design consideration based on wide output voltage range for the second stage of an on-board battery charger is discussed. The output voltage range is determined with the series connection of enough lithium-ion battery cell. According to lithium-ion battery charge characteristic, soft switching and efficiency performance of PSFB converter over wide output voltage range is evaluated. The optimum operation point to maintain soft switching operation of the converter for wide output voltage range is determined. To validate theoretical evaluations, a prototype operating at 200 kHz and regulating output voltage between 42 V and 54 V, is built in laboratory. The soft switching operation and the output regulation of the converter is tested for wide output voltage range.

II. BASIC PRINCIPLES OF PSFB CONVERTER

The circuit scheme of PSFB PWM converter is shown in Fig. 1. S_1–S_4 are the primary MOSFETs, D_{R1} and D_{R2} are rectifier diodes, L_m is the magnetizing inductance, and L_s is the snubber inductance which includes leakage inductance of the transformer and extra added inductance. L_o is the output filter inductor and C_o is the output filter capacitor. V_{in} is the input voltage source, V_o is the battery voltage, N is the turns ratio of the transformer. The theoretical key waveforms of the converter are also given in Fig. 2.

In the powering stages, S_1-S_2 or S_3-S_4 are turned on and that two MOSFET pairs share one switching period. During the conduction of S_1 and S_2, at t=t_0, the input voltage is applied to the primary side of the transformer, and the primary current increases linearly. At the secondary side, DR_2 is on and the power is transferred to the output. The primary current change can be written as follows:

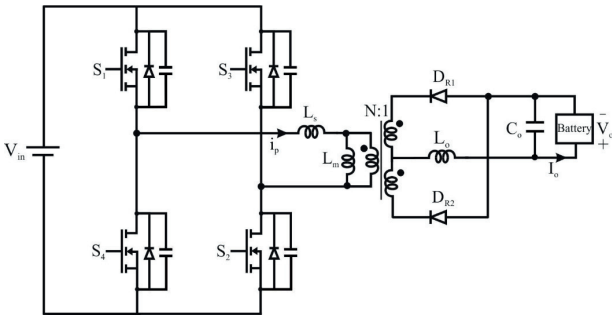$$\frac{di_p}{dt} = \frac{V_{in} - V_o'}{(L_o' + L_s)}, \qquad (1)$$

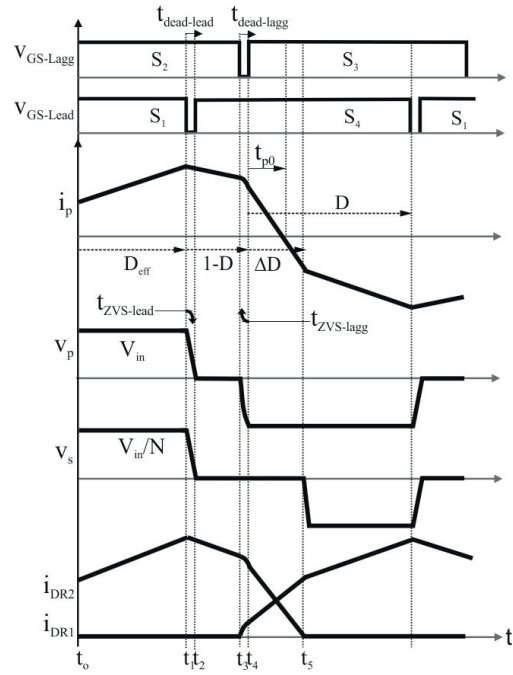Figure 1. The circuit schematic of PSFB converter.

Figure 2. The theoretical key waveforms of PSFB PWM converter.

where V_o' and L_o' represent the reflected output voltage and the output filter inductor to the primary side. Then, at t=t_1, S_1 is turned off, and the parasitic capacitors of S_1 and S_4 MOSFETs are charged and discharged by the reflected output current. At t=t_2, the antiparallel diode of S_4 MOSFET turns on when the voltage of the parasitic capacitor of S_4 reaches zero. Thus, freewheeling mode starts and the primary windings of the transformer are short circuited. DR_2 is still on and conducts the output current. To achieve ZVS turn on for S_4 MOSFET, control signal to be turned on S_4 should be applied during in the freewheeling mode. The primary current change for freewheeling mode can be written as

$$\frac{di_p}{dt} = \frac{V_o'}{L_o' + L_s}. \qquad (2)$$

Then, at t=t_3, S_2 is turned-off and so the parasitic capacitors of S_2 and S_3 MOSFETs are charged and discharged. At the secondary side, the output current commutation starts between DR_1 and DR_2 by the conduction of DR_1. Thus, secondary windings of the transformer is short circuited and so the output current cannot be reflected to the primary side. Therefore, L_s inductance should provide required energy to discharge and charge the parasitic capacitors of the lagging leg switches since there is no current reflected from the output. If the parasitic capacitor of S_3 discharges completely, its antiparallel diode turns-on and ZVS turn-on of S_3 is achieved at t=t_4. Then, the negative input voltage is applied to the primary side of the transformer. At the secondary side, the output current commutation continues and the secondary windings of the transformer are still short circuited. If the charge and the discharge time interval of parasitic capacitors are neglected, the primary current change

for the output current commutation can be written as follows:

$$\frac{di_p}{dt} = -\frac{V_{in}}{L_s}. \tag{3}$$

The output current commutation interval causes lost duty cycle, ΔD, since no energy is transferred from the input to the output. This situation can be defined approximately as

$$\Delta D \approx \frac{2I_o L_s f_s}{N V_{in}}. \tag{4}$$

Where f_s is the switching frequency, and I_o represents the output current. Thus, as shown in Fig. 2, effective duty ratio D_{eff} can be defined as

$$D_{eff} = D - \Delta D. \tag{5}$$

Where D is the total duty time applying the switches. The half switching period is completed when the output current commutation is completed at t=t_5. The remaining half cycle works with the same principle but inverse direction of the primary current and voltage.

A. ZVS Requirements of Leading Leg MOSFETs:

The soft switching operation of leading leg MOSFETs (S_1 and S_4) can be achieved easily with the reflection of output current to the primary side and optimized dead time. The dead time requirement for leading leg MOSFET can be defined as

$$t_{dead-lead} \geq t_{d(off)} + t_{rv}. \tag{6}$$

Where $t_{d(off)}$ represents the turn-off delay time and t_{rv} defines the voltage rising time obtained from datasheet of primary MOSFETs. The duration of charge/discharge of parasitic capacitors defines the ZVS interval and it can be extracted as follows:

$$t_{ZVS-lead} = \frac{(C_{S1} + C_{S4})V_{in}}{I_{p-t1}}. \tag{7}$$

The dead time should be enough to allow charge and discharge of the parasitic capacitors so dead time for leading lead MOSFETs is also defined as

$$t_{ZVS-lead} \leq t_{dead-lead}. \tag{8}$$

B. ZVS Requirements of Lagging Leg MOSFETs:

The soft switching operation of lagging leg MOSFETs depends on load condition and it can get poor at light load conditions. Because short circuit condition of secondary windings removes the reflection of the output current to the primary side and

so stored energy in L_s should provide discharge and charge the parasitic capacitors of the lagging leg switches. This condition can be defined as

$$\frac{1}{2}L_s I_{p-cr}^2 \geq \frac{1}{2}(C_{S2} + C_{S3})V_{in}^2. \tag{9}$$

Where, I_{p-cr} defines the required minimum primary current to be charged and discharged the parasitic capacitors of lagging leg MOSFETs and $(C_{S2}+C_{S3})$ represents the equivalent parasitic capacitors during the resonance occurred between L_s and parasitic capacitors.

The dead time requirement of lagging leg MOSFETs is different compared to leading leg MOSFETs. The dead time should be enough to charge and discharge of parasitic capacitors as follows:

$$t_{dead-lagging} \geq t_{d(off)} + t_{rv}. \tag{10}$$

In addition, the dead time also should be ended before primary current falls to zero to prevent reverse resonance and recharge the parasitic capacitors [16], [17]. This can be defined as

$$t_{ZVS-lagg} \leq t_{dead-lagg} \leq t_{p0}. \tag{11}$$

Where $t_{ZVS-lagg}$ is the charge and discharge time of the parasitic capacitors of the lagging leg MOSFETs. The duration of the charge and the discharge of the parasitic capacitors defines the ZVS interval and it can be extracted from the equivalent series resonant circuit as follows:

$$t_{ZVS-lagg} = \sqrt{L_s(C_{S2} + C_{S3})}\, tg^{-1}\frac{V_{in}}{I_{p-t3}}\sqrt{\frac{C_{S2} + C_{S3}}{L_s}}. \tag{12}$$

Where t_{p0} is the time duration which the primary current falls to zero in as shown in Fig. 2 and it can be written as

$$t_{p0} = \sqrt{L_s(C_{S2} + C_{S3})}\, tg^{-1}\frac{V_{in}}{I_{p-t3}}\sqrt{\frac{C_{S2} + C_{S3}}{L_s}} + L_s\frac{I_{p-t4}}{V_{in}}. \tag{13}$$

III. PERFORMANCE ANALYSIS OF PSFB PWM CONVERTER BASED ON WIDE RANGE OUTPUT VOLTAGE REGULATION

In this section efficiency optimization of PSFB converter based on wide range output voltage regulation is discussed. For the output of converter, 14 battery cells connected as series are assumed. According to lithium-ion battery charge characteristic given in Fig. 3 [11], the voltage of a battery cell changes between 3.1 V and 3.85 V. To evaluate the performance of PSFB converter, several points are addressed on the charge characteristic of li- ion battery
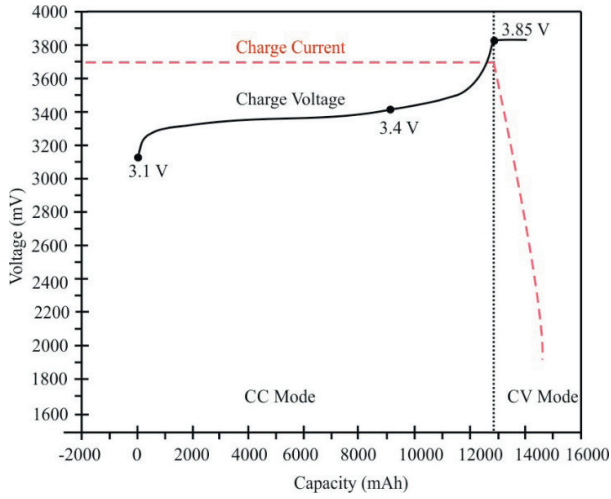
Figure 3.   Lithium-ion battery charge characteristic.

cell, given in Figure 3. Four operation points of the battery cell are 3.1V/15A, 3.4V/15A, 3.85V/15A and 3.85V/3A. Thus, according to assumption of series connection of 14 battery cell, the output voltage range of PSFB converter is changed from 43.4 V to 53.9 V.

According to soft switching operation conditions of PSFB converter discussed earlier, ZVS turn-on operation of the primary MOSFETs are evaluated for determined output voltage range of battery package. The evaluation should be took into consideration the dead time requirements because duty ratio and so dead time also varies to regulate the output voltage range. The soft switching operation of leading leg MOSFETs is not affected by varying dead time. The varying dead time affects the soft switching operation of the lagging leg MOSFETs. Thus, the dead time optimization of lagging leg over wide output voltage range is discussed in this work. Therefore, the dead time requirement condition for the lagging leg switches is firstly defined.

For the performance analysis, SiC CMF20120D is used as primary MOSFET. According to the rising and falling time obtained from the MOSFET's datasheet, dead time of the lagging leg MOSFETs is calculated as 78 ns based on equation (10). The ZVS time interval is calculated as 77 ns based on (12). The time interval, which primary current falls to zero, is obtained as 137 by the use of (13). Thus, following condition should be provided to achieve ZVS turn-on of lagging leg switches.

$$77\,ns < t_{dead-lagg} < 137\,ns \qquad (13)$$

In the calculation results given above, L_s inductance is selected as 10 µH and the equivalent parasitic capacitor of lagging leg MOSFETs, C_{lagg}, is obtained as 2x120 pF from MOSFET's datasheet. According to dead time requirements, the evaluation results are obtained for constant current operation as given in Table I. The lagging leg MOSFETs of the converter turns-on with ZVS just at 54 V and they turn-on hardly at the other voltage points since effective duty ratio becomes smaller and dead time is larger. This results in reverse resonance which charges

the parasitic capacitor of MOSFETs to the input voltage.

To extend the soft switching operation for wide range output voltage regulation, the value of the snubber inductance, L_s, can be increased but this also increases the lost duty ratio power losses, namely conduction loss occurred during the output current commutation of PSFB converter. In order to see effects of L_s snubber inductance on soft switching operation of lagging leg MOSFETs and the conduction loss, a calculation study is performed in Matlab. The dead time change as function of L_s and based on full load condition is given in Fig. 4. The maximum extension of time interval, t_{p0}, is limited by 24 µH to provide output voltage regulation while the turns ratio of transformer is 6. If the turns ratio is reduced, the further extension of t_{p0} is possible but this also results in the increased conduction loss. Therefore, the evaluation procedure is continued with 6 turns ratio. The primary current falls to zero in 263 ns if L_s inductance is selected as 24 µH as shown in Figure 4. However, at this point, the calculated t_{ZVS} value not provides the required condition for ZVS turn-on of the lagging leg MOSFET because t_{ZVS} should be smaller than dead time, over wide load range, given in Table 1. If L_s is selected 20 µH, the required conditions for t_{ZVS} and t_{p0} are provided. This operation point provides soft switching operation from 50 V to 54 V.

TABLE I.   SWITCHING OPERATION OF THE LAGGING LEG MOSFETs BASED ON WIDE RANGE OUTPUT VOLTAGE.

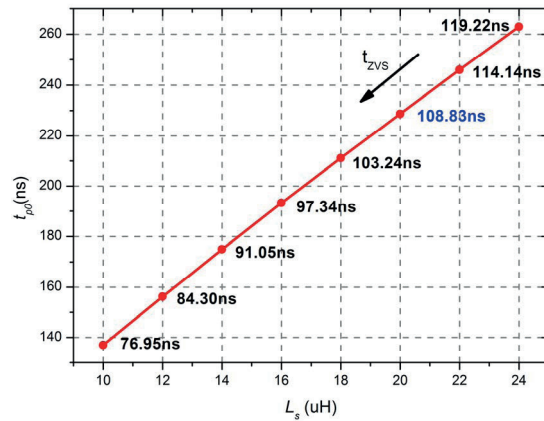| I_o=15 A, V_{in}=385 V, L_s=10 µH, C_{lagg}=240 pF, n=6			
Vo	$t_{dead-lagg}$	D_{eff}	Turn-on Sw.
42	362.5 ns>tp0	0.71	Hard
44	325 ns>tp0	0.74	Hard
46	275 ns>tp0	0.78	Hard
48	237.5 ns>tp0	0.81	Hard
50	200 ns>tp0	0.84	Hard
52	150 ns>tp0	0.88	Hard
54	112.5 ns<t$_{p0}$	0.91	ZVS

Figure 4.   The change of t_{p0} based on the variation of L_s.

IV. EXPERIMENTAL RESULTS

The presented design procedure of PSFB converter for on-board EV battery chargers is validated by a prototype. The nominal 385 V dc input voltage is applied to the primary side of the converter. The converter is operated for 42-54 V / 15 A output at 200 kHz switching frequency. The power semiconductors and the magnetic components used in the prototype are given in Table II. In the performance evaluation of the converter, ZVS turn-on of lagging leg MOSFETs were evaluated.

Fig. 5 provides the drain-source voltage of S_2 MOSFET and the primary current with 54 V / 15 A output. For the maximum output voltage of the battery package, ZVS turn-on of the lagging leg MOSFET, S_2, is validated with the measured results.

The soft switching operation of S_2 MOSFET is also measured for 50 V output voltage at full load condition and the measured waveforms are given in Fig. 6. Measured results shows that ZVS turn-on of lagging leg MOSFETs is maintained at 50 V.

Fig. 7 provides the measured results while the output voltage is 48 V with full load condition. As anticipated, soft switching operation of lagging leg switches are lost.

TABLE II. THE USED COMPONENTS IN THE PROTOTYPE.

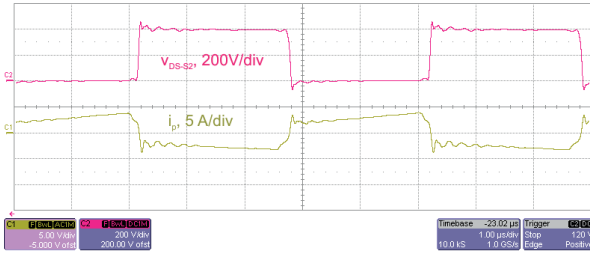| Parameters	Values
S_1-S_4	SiC C2M0080120
D_{R1}-D_{R4}	DSS2x101-015A
TR	E/65/32/27, N_p=12, N_s=2
L_r	20 µH home made
L_o	1.1 µH home made
C_o	12x22 µF ceramic capacitor

Figure 5. The drain-source voltage of S_2 MOSFET (v_{DS-S2}), the primary current (ip) at V_o=54 V, I_o=15 A, f_s=200 kHz and V_{in}=385 V.
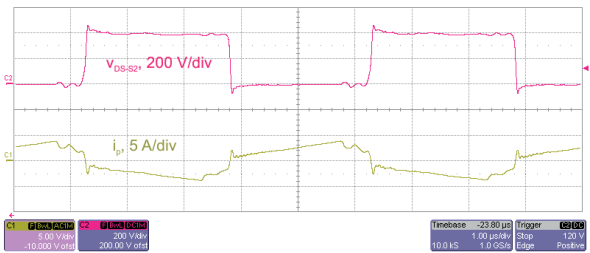

Figure 6. The drain-source voltage of S_2 MOSFET (v_{DS-S2}), the primary current at V_o=50 V, I_o=15 A, f_s=200 kHz and V_{in}=385 V.
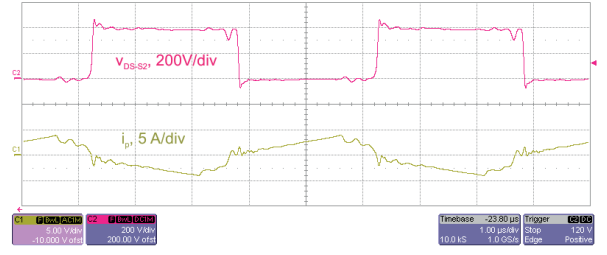

Figure 7. The drain-source voltage of S_2 MOSFET (v_{DS-S2}), the primary current at V_o=48 V, I_o=15 A, f_s=200 kHz and V_{in}=385 V.

Fig. 8 gives the measured efficiency results based on battery voltage with 15 A constant current. The measured maximum efficiency was obtained as 94.4% with 54 V/15 A output. The efficiency decreases while the battery voltage decreases because ZVS turn-on operation is not maintained under 50 V and also output power is decreased.
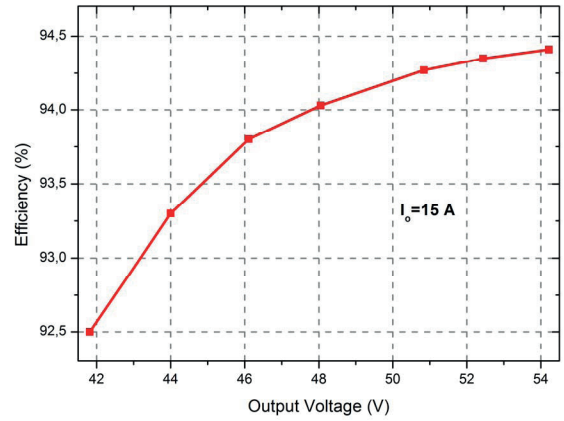

Figure 8. The measured efficiency values as function of battery voltage.

V. CONCLUSIONS

In this study, the soft switching operation of PSFB converter is discussed based on wide range output voltage of EV battery chargers. The soft switching requirements of the lagging leg MOSFETs are taken into consideration to evaluate effects of the duty ratio varying to regulate 42-54 V output voltage range. The snubber inductance value is optimized to 20 µH to reach high efficiency over wide output voltage range. The obtained theoretical results are validated with a prototype built with 42-54 V/15 A at 200 kHz. The efficiency variation based on battery voltage range with constant output current was also extracted. The maximum efficiency is measured as 94.4% with 54 V/15 A output.

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