NEON: Near-Accurate Efficient FIR Filter for Ultra Low-Power Applications

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***Abstract*—Low-power dissipation is an imperative requirement in the design of an efficient Digital Signal Processing system which is employed in many multimedia applications such as image and video processing. Finite Impulse Response (FIR) filter is indispensable in the design of several such Digital Signal Processing (DSP) applications. The output of these applications, either an image or a video can be nearly accurate for human perception. This toleration in the loss of quality of the output can be exploited to design an energy-efficient system by using approximate computation. Moreover, the efficacy of a system can be improved multi-fold by using reversible logic which benefits in the design of ultra-low-power systems. In this paper, we propose an approximate adder using a reversible Toffoli gate and employ it in designing NEON (Near-accurate and Efficient FIR filter for ultra low-power applicatiONs). Simulation results carried out using Cadence© design tools in 45nm technology node show that the FIR Filter designed using the proposed adder gives significantly better results compared to the designs using the adders in literature. Experiment results using ISCAS benchmarks and comparison with previous methods demonstrate the effectiveness of the proposed method. In addition to producing fewer garbage outputs, the FIR filter designed using the proposed adder yields power reduction of 74%, delay reduction of 64% and Power-Delay Product reduction of 90.1%.**

I. Introduction

Typically used multimedia applications involving image or video processing have Digital Signal Processing blocks as the backbone. Finite Impulse Response (FIR) filters are widely used in these applications. The resultant output, usually an image or a video, can be nearly accurate for human perception. This relaxation on producing strictly accurate outputs facilitates in carrying out approximate computation. This flexibility can be utilized in designing low-power systems.

Earlier works targeting design of low-power systems using proximate computations include Algorithmic Noise Tolerance (ANT) [1-4] which focus on limiting the errors by using the concept of Voltage Over-Scaling. A low-power approximate adder is proposed in [5], which functions by separating the inputs into accurate and approximate parts. Probabilistic Computing has been proposed as an alternative in [6-8] which produces inexact outputs in order to achieve less power consumption and hardware complexity. Various inaccurate adders have been proposed in [9-10] which embrace error to achieve reduced power dissipation. An imprecise specification has been proposed in [11] which focuses on improving RTL specification by adding new semantic elements. Woo[12] has proposed an analog adder using approximate computation.

Of late, reversible logic has emerged as a paradigm in designing energy-efficient systems. Landauer [13] has proved that for irreversible logic computations, every bit of information lost results in the generation of KT log2 joules of heat energy. Bennet [14] showed that this heat dissipation would not occur in reversible computation. Several reversible gates have been proposed such as Fredkin Gate [15], Toffoli Gate [16] and Feynman Gate [17-18]. Low-power adder circuits are designed using a new reversible gate proposed in [19]. Using reversible gates, several adders and multipliers are designed in [20-30] which dissipate low-power. An FIR filter model is designed using reversible logic gates in [33]. In [34], an ultra low-power FIR filter is proposed using subthreshold design approach. One of the important concerns in designing a reversible logic system is to use as few reversible logic gates as possible and produce fewer number of garbage outputs.

FIR filters use several addition operations. To design an energy-efficient low-power FIR filter, it is imperative to design low-power adder cells. Our approach is described as follows: First, an approximate full adder cell is designed using reversible logic. This adder cell is later utilized in the design of an FIR filter (NEON).

Despite the emergence of several approximation algorithms, limited amount of work has been focused on approximating FIR Filters. Previous work [33] presents the design of FIR Filter using reversible Fredkin gates. However, this design produces many garbage outputs and consumes a lot of power and thereby presents hindrance to the design of an efficient Digital Signal Processing system. To the best of our knowledge, this work presents the first approximate reversible adder which not only produces minimal garbage outputs but also yields significant reductions in terms of power, delay and Power-Delay Product.

The remainder of the paper is organized as follows. Section II outlines previous work related to the emergence of Approximation Algorithms and Reversible Logic. In section III, an approximate full adder using reversible logic gates is presented. In section IV, we propose NEON. In section V, we compare NEON with the design of FIR filters using existing adders

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in terms of power, delay and Power Delay Product (PDP). Section VI concludes the paper.

II. Previous Work

Approximate Computing has emerged as a paradigm shifting technique in the design of ultra low-power systems whose applications can tolerate error. Of all the techniques proposed previously, we make use of Logic Complexity Reduction technique which minimizes the Boolean Expressions [9-11] resulting in reduced hardware overhead and thereby CPU time.

A. Reversible Logic

Reversible Logic bestows in carrying out low-power computations. Irreversible logic computations result in the dissipation of KT log2 joules of heat energy for every bit of information lost. In reversible systems, the aforementioned heat dissipation would not occur as the system's input vectors can be retrieved from output vectors. There is a one-to-one correspondence between input and output assignments [13-14] in reversible systems. Hence, an input vector (I) can be uniquely obtained from the output vector (O) in a reversible system. Block diagram of a reversible system is shown in Fig. 1. below.

Fig. 1. Reversible System

A $k \times k$ reversible gate can be represented as:

$$I = (I_0, I_1 \ldots\ldots I_{k-1}, I_k) \tag{1}$$

$$O = (O_0, O_1 \ldots\ldots O_{k-1}, O_k) \tag{2}$$

We propose the design of approximate Full-Adder cell using a reversible Toffoli gate.

B. Toffoli Gate

Toffoli Gate is a 3 X 3 Reversible Gate with input and output equations as follows [16]:

$$I = (A, B, C) \tag{3}$$

$$O = (A, B, AB \oplus C) \tag{4}$$

The block diagram of Toffoli Gate is shown in Fig.2.

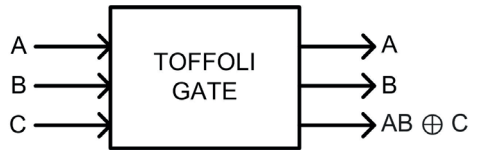

Fig. 2. Toffoli Gate

III. Novel Proposed Approximate Adder

In this section, the design of a low-power Approximate Full-Adder cell is discussed. A close examination of the truth table of a conventional Full Adder shows that Sum = B and C_{out} = A for 4 cases out of 8. As shown in Table I, for the input combinations A = 0, B = 0, C_{in} = 0 ; A = 0, B = 1, C_{in} = 0 ; A = 1, B = 0, C_{in} = 1 and A = 1, B = 1, C_{in} = 1, the approximated Full Adder's output is similar to that of a conventional Full Adder.

TABLE I. Truth table for conventional Full Adder and Approximated Adder

Inputs			Accurate Outputs		Approximate Outputs	
A	B	C_{in}	Sum	C_{out}	Sum_a	C_{outa}
0	0	0	0	0	0√	0√
0	0	1	1	0	0×	0√
0	1	0	1	0	1√	0√
0	1	1	0	1	1×	0×
1	0	0	1	0	0×	1×
1	0	1	0	1	0√	1√
1	1	0	0	1	1×	1√
1	1	1	1	1	1√	1√

Sum = B and C_{out} = A.

The above equation is implemented using a standard Toffoli gate to design the Proposed Adder which is presented in Fig. 3. The Gate level structure of the Proposed Adder is shown in Fig. 4.

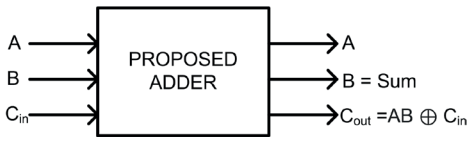

Fig. 3. Proposed Approximate Reversible adder

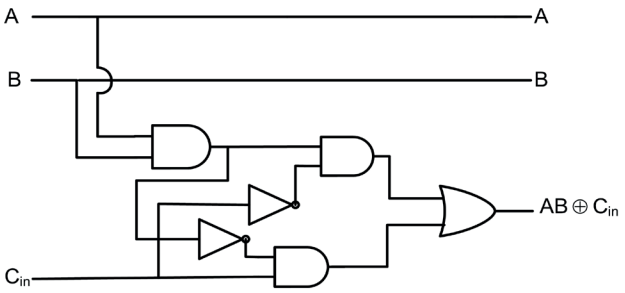

Fig. 4. Gate level Structure of the Proposed Adder

To evaluate the efficacy of the proposed design, we compare the Proposed Adder with reversible full adders and with approximate adders in the literature. These comparison results are presented in Table II. It can be observed that the proposed adder yields better results in terms of power and number of garbage outputs compared to adders existing in the literature.

IV. Design of NEON using the Proposed Approximate Adder

In the previous section, the design of the Proposed Approximate Adder was presented and its efficiency in terms of Power, Delay and Power-Delay Product was compared with the existing design in the literature. In this section, the design of NEON (FIR Filter), which

TABLE II. PERFORMANCE EVALUATION OF THE PROPOSED ADDER IN TERMS OF POWER AND NUMBER OF GARBAGE OUTPUTS

Design	Reversibility	Technique	Power(nW)	Garbage Outputs
Md.Azad khan [30]	√	Accurate	4218.991	4
HNG Gate [28]	√	Accurate	3577.672	2
Multiplexer based FA [31]	√	Accurate	2513.752	3
IC Approx 1 [9]	×	Approx	2969.419	NA
IC Approx 2 [9]	×	Approx	2432.521	NA
IC Approx 3 [9]	×	Approx	1911.338	NA
IC Approx 4 [9]	×	Approx	1483.64	NA
XOR/XNOR Approx 1 [10]	×	Approx	1460.59	NA
XOR/XNOR Approx 2 [10]	×	Approx	2163.708	NA
XOR/XNOR Approx 3 [10]	×	Approx	1374.963	NA
Novel Proposed Adder	√	**Approx**	**1148.186**	**1**

is widely used in many multimedia applications is presented using the Proposed Approximate Adder.

A. Finite Impulse Response (FIR) Filter

FIR filters are extensively used in many Digital Signal Processing systems intended for multimedia applications. The schematic of a typical FIR filter is presented in this section. An FIR Filter produces a finite impulse response. For a causal discrete-time FIR filter of order 'N', each value of the output sequence is a weighted sum of most recent input values. The mathematical representation of a causal discrete-time FIR Filter is presented below.

$$y[n] = b_0 x[n] + b_1 x[n-1] + \ldots + b_n x[n-N] = \sum_{i=0}^{N} b_i.x[n-i]$$

Where x[n] is the input signal, y[n] is the output signal, 'N' is order of the filter and b_i is the value of impulse response at i^{th} instant for $0 \leq i \leq N$. Input data is multiplied with the filter coefficients and the summation of the results provide the filter response. An FIR filter of 'Nth' order requires 'N' summations.

In the design of the proposed FIR filter, all conventional adders are replaced by the Proposed Adder cells. FIR filter structures for 8, 12 and 16 orders are designed. The design of an 'N'th order NEON using the Proposed Adder cells is shown in Fig. 5.

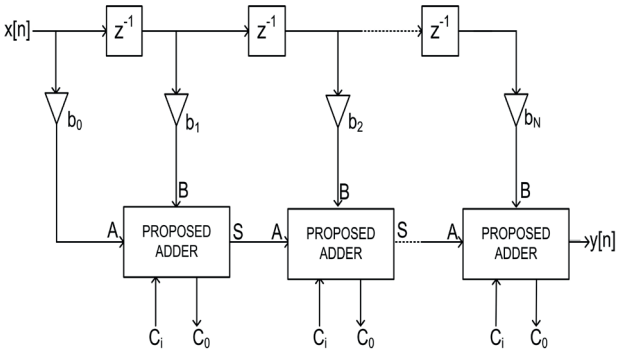

Fig. 5. Design of NEON using the Proposed Adder cells

V. EXPERIMENTAL RESULTS

To demonstrate the efficacy of the proposed adder, we have compared its performance with the adders existing in literature [9-10, 30]. The simulation results are carried out using ISCAS Benchmark Suite[35] and the results are very encouraging. These results are tabulated in Table III.

A. Performance Evaluation of NEON

In this section, we compare the efficiency of 8, 12 and 16 order NEON with the FIR Filters using existing adders [9, 30-31]. We have embedded each of these adders in designing the FIR Filter (Fig. 5.) and implemented them using Verilog HDL for 8,12 and 16 bit widths of input numbers. We have implemented the aforementioned designs and synthesized them using Cadence design tools at 45nm technology node. The performance of NEON in terms of Power, Delay and Power-Delay Product (PDP) is considered with respect to the bit width of the input numbers.

1) Analysis of FIR Filter in terms of Power Dissipation: The performance of NEON in terms of power dissipation for various orders of 8, 12 and 16 has been tabulated in Table IV. As the proposed adder produces only one garbage output, the power dissipation of NEON is very much less when compared to FIR filter using existing adders in literature [9, 30-31]. Fig. 6. depicts the average power dissipation measurements of 8, 12 and 16 order NEON over the FIR Filter using existing adders[9, 30-31].

TABLE IV. TOTAL AVERAGE POWER DISSIPATION OF FIR FILTER OF ORDERS 8, 12 AND 16

Design	Power (mW)		
	Order 8	Order 12	Order 16
Azad Khan[30]	10.49	29.50	57.32
Thapliyal[31]	9.25	25.48	50.81
Allen [9], Approx4	4.31	11.37	20.66
Proposed Method	**1.15**	**1.75**	**2.36**

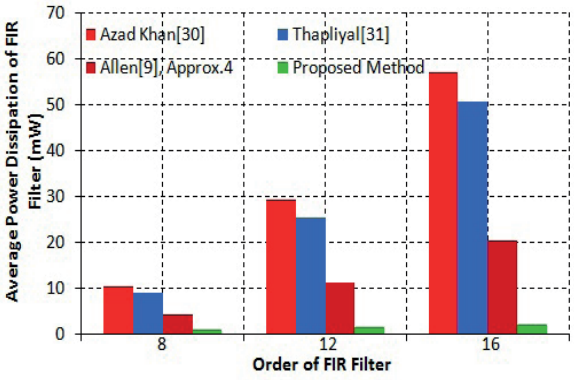

Fig. 6. Total Average Power Dissipation of FIR Filter of orders 8, 12 and 16

2) Analysis of FIR Filter in terms of Delay: Table 5 presents the performance of NEON in terms of delay savings for FIR Filters of order 8, 12 and 16. As the design of the Proposed Adder utilizes only a single

TABLE III. EXPERIMENT RESULTS USING ISCAS BENCHMARKS[35] (POWER(MW), CPU TIME(NS), PDP(FJ))

Circuit	Yang[10],Approx 3			Allen[9],Approx 4			Azad Khan[30]			Proposed Method		
	Power	CPU Time	PDP	Power	CPU Time	PDP	Power	CPU Time	PDP	Power	CPU Time	PDP
c1908	84.21	62.31	5.25	85.05	62.93	5.35	85.9	63.56	5.46	32.12	22.14	0.71
c2670	88.42	77.26	6.38	98.14	85.76	8.42	108.94	95.19	10.37	33.21	23.89	0.79
c5315	149.43	78.03	11.66	185.29	96.75	17.93	229.76	119.97	27.56	72.10	35.41	2.55
c3540	170.35	104.56	17.81	223.16	136.97	30.57	292.34	179.43	52.45	81.20	39.29	3.19
c6288	272.56	140.12	38.19	395.21	203.17	80.29	573.05	294.59	168.81	110.32	58.42	6.44
c7552	327.07	346.10	113.19	755.53	799.49	604.04	1745.27	1846.82	3223.19	152.39	63.81	9.72
s9234	346.69	508.77	176.39	429.89	630.87	271.20	533.06	782.28	417.002	154.97	78.89	12.23
s13207	741.93	1190.53	883.29	875.47	1404.83	1229.89	1333.05	1657.69	1712.47	256.39	103.92	26.64
s15850	1187.09	1214.34	1441.53	1424.50	1457.21	2075.79	1709.4	1748.65	2989.14	398.31	123.51	49.19
s35932	1424.51	1408.63	2006.61	1709.41	1690.36	2889.52	2051.28	2028.43	4160.87	412.97	169.99	70.20
s38417	1908.84	2366.50	4517.27	2290.6	2839.8	6504.85	2748.72	3407.76	9366.97	627.14	193.21	121.17
s38584	3206.86	4685.68	15026.32	3848.16	5622.7	21637.05	4617.79	6747.24	31157.34	721.98	202.43	146.15

reversible gate, lesser delay is obtained for NEON compared to the FIR filter using existing adders in literature [9, 30-31]. The delay measurements of 8, 12 and 16 order NEON over the FIR filters designed using existing adders [9, 30-31] is presented in Fig. 7.

TABLE V. DELAY OF FIR FILTER WITH ORDERS 8, 12 AND 16

Design	Delay (ns)		
	Order 8	Order 12	Order 16
Azad Khan[30]	11.00	11.41	17.37
Thapliyal[31]	9.93	10.16	16.47
Allen [9], Approx4	6.05	8.02	10.61
Proposed Method	**2.38**	**2.39**	**2.78**

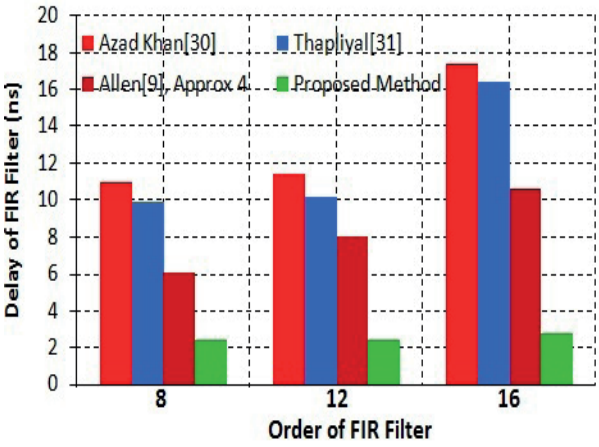

Fig. 7. Delay of FIR Filter of orders 8, 12 and 16

3) Analysis of FIR Filter in terms of Power-Delay Product (PDP): In Table VI, the utility of NEON in terms of Power-Delay Product (PDP) savings is shown. PDP measurement determines the energy-efficiency of a system. Savings in terms of Power and Delay of NEON benefits in the reduction of Power-Delay Product as well. Table VI depicts that the PDP of NEON is less compared to FIR filter using adders in [9, 30-31]. PDP measurements of 8, 12 and 16 order NEON over the FIR filter using adders in literature [9, 30-31] is shown in Fig. 8.

TABLE VI. POWER DELAY PRODUCT OF FIR FILTER WITH ORDERS 8, 12 AND 16

Design	Power Delay Product (pJ)		
	Order 8	Order 12	Order 16
Azad Khan[30]	115.39	336.59	995.64
Thapliyal[31]	91.85	249.70	836.84
Allen [9], Approx4	26.07	91.18	218.996
Proposed Method	**2.73**	**4.18**	**6.56**

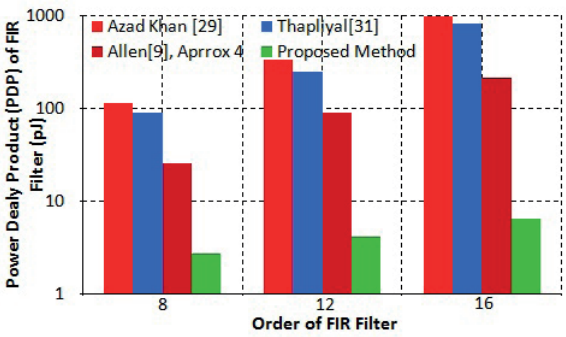

Fig. 8. Power Delay Product of FIR Filter of orders 8, 12 and 16

VI. CONCLUSIONS

In this paper, we have proposed an Approximate Reversible Adder and analyzed its performance in FIR Filters of various orders. Our approach is aimed at achieving an ultra-low power design of FIR Filter with minimal garbage outputs. We have compared the performance of Proposed Adder in terms of power, delay and PDP with reversible adders and approximate adders in literature. Usage of the Proposed Adder in designing FIR Filters of 8, 12 and 16 orders yielded significant reduction in terms of power, delay and PDP in comparison with the FIR filters designed using adders in the literature.

VII. ACKNOWLEDGEMENT

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