A New Soft Switching Bridgeless PFC Converter With Lossless Snubber

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Abstract – Increasing use of rectifiers causes harmonics pollution in networks. So use of power factor correction (PFC) in converters is inevitable. For reducing weight and volume of converters, designers try to increase switching frequency. The switching losses and conduction losses are two sources of losses in the switching power converter. Thus to reduce these losses, a new bridgeless soft switching PFC converter without any extra switch is introduced in this paper. A passive lossless snubber is used for bridgeless boost converter which can reduce the switching and conduction losses simultaneously. The proposed converter provides soft switching condition for all semiconductor elements. The proposed converter is analyzed theoretically and the design consideration are given. Then for a design example, the values of circuit elements are calculated. It is simulated by PSIM. Finally the efficiency comparison that is simulated by ORCAD software is presented. It shows that the proposed converter improve the efficiency at the nominal load in comparison with hard switching counterpart.

Keywords- Boost PFC Converters; Bridgeless; Lossless Snubber; Soft Switching.

I. INTRODUCTION

Nowadays, most of the electronic devices need a DC voltage power supply. Typically, the conventional diode bridge is used for AC/DC conversion. The main problems of bridge diode are non-sinusoidal input current waveform and harmonic pollution. To limit the current harmonics and improve the power factor, the power factor correction circuits can be used [1]. Therefore, many surveys have been done to improve the performance and efficiency of the PFC circuits.

The bridge rectifier followed by a DC/DC converter makes an active PFC circuit. Various DC/DC converter can be used. The boost converter is the conventional converter that is used in PFC converter. It has lower cost, simple structure and higher performance in comparison with the other proposed structures [2]. This converter also has disadvantages such as following. (1) Isolation between input-output is difficult, (2) Peak of the input voltage is always lower than the output voltage, (3) The inrush current at the start up is high, (4) There is no current limitations at the overload conditions [3]. Various topologies of basic PFC are compared in [4].

To reduce the conduction losses, various methods are used such as bridgeless and single stage PFC converters. The bridgeless PFC converters can be used in any applications which need a DC bus voltage.

Recently, to increase the efficiency of the boost PFC converters, soft switching techniques has been applied [5-6]. Soft switching techniques reduce the switching losses [7-12]. These techniques can be classified into two categories, zero current switching (ZCS) and zero voltage switching (ZVS). ZCS technique is proper to be implemented with IGBTs where the tailing current can be removed, while ZVS technique is proper to be applied with MOSFETs to remove the turn-on capacitive losses [13]. Other types of soft switching converters are employed by using active and passive snubbers [14]-[15]. Commonly by adding an extra switch to the passive snubbers, Active snubbers are made which are called ZVT or ZCT soft switching circuit. So the complexity of the controller is increased to provide extra switch gate signal. Also these converters usually have extra voltage or current stresses on the main semiconductor elements. But in the passive snubber circuits there are not any extra switch. Therefore the complexity of the controller does not increase. Usually these circuits provide ZCS condition for turning on instant and ZVS condition for turning off instant. It must be noted that in these two method, the control of the converter is PWM.

In this paper a new bridgeless soft switching PFC converter without any extra switch is introduced which can provide ZVS condition at turning off instant. The proposed converter simultaneously uses bridgeless PFC for reducing conduction losses and passive snubber for reducing switching losses. So better efficiency can be achieved. This paper is organized in five sections. In the next section, the theatrical operation of the proposed converter is analyzed in details and in section III based on the converter operation, the designing of the proposed converter is presented. Section IV shows the simulation results that confirm the theoretical analysis.

II. PROPOSED CONVERTER AND THEORETICALLY ANALYSIS

The proposed PFC converter is shown in Fig.1 that consists of two boost converters and operates in each half line cycle. Switches S_1 and S_2, Diodes D_5 and D_6 and Inductor L_1 are the main components of two boost converter. The other elements make a passive lossless snubber to provide soft switching condition. The

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proposed snubber can provide ZVS condition for S_1, S_2 and other semiconductor elements in the circuit.

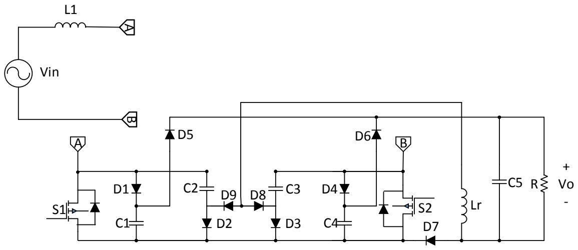


Figure 1. The proposed boost converter

The operation of the proposed converter is symmetrical in two half line cycles. So operation of the proposed converter is just explained in positive half line cycle. It is also assumed that the proposed converter operation is in CCM (Continuous Conduction Mode). The body diode of S_2 switch is ON at all modes. Also the input inductor and output capacitor are assumed large enough. thus in a switching cycle, these can be replaced by I_{in} current source and V_{out} voltage source respectively. Based on the above assumption the equivalent circuit model in positive half line cycle and a switching cycle is shown in Fig.2. This converter has 4 operation modes. Fig. 3 shows the equivalent circuits of each operation mode and Fig. 4 shows theoretical key waveforms of the proposed converter. It is assumed that before t_0, S_1 and the body diode of S_2 is on, and capacitors C_1, C_2 are discharged to zero value and diodes $D_1 \sim D_7$ are OFF.

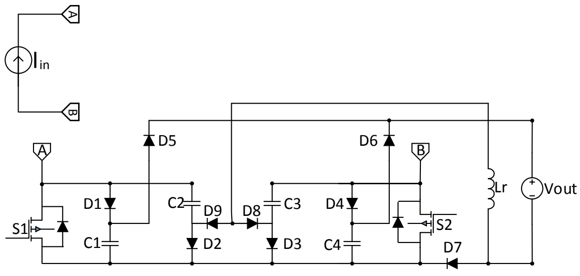


Figure 2. Equivalent circuit model of the proposed boost converter

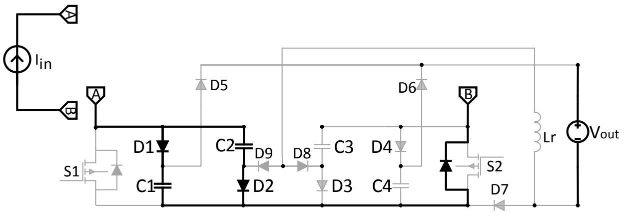
A. Mode 1 ($t_0 < t < t_1$)

At t_0, the switch S_1 is turned off, thus diodes D_1 and D_2 are begin to conduct under ZVS condition. The inductor L_1 starts to charge capacitors C_1 and C_2. Since in this mode C_1 and C_2 are placed parallel with S_1, the switch S_1 turned off under ZVS condition. The C_1 capacitor voltage can be calculated from (1). This mode lasts until the voltage of C_1 and C_2 reaches to V_O. therefore the duration of this mode can be calculated by (2):

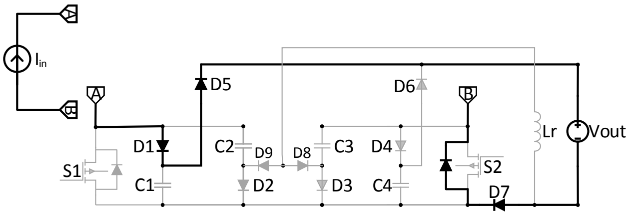
$$V_{C1}(t) = V_{C2}(t) = \left(\frac{I_{in}}{C_S}\right) \times (t - t_0) \tag{1}$$

Where $C_S = C_1 + C_2$

$$t_1 = \frac{I_{in}}{C_S . V_O} + t_0 \tag{2}$$



STAGE 1



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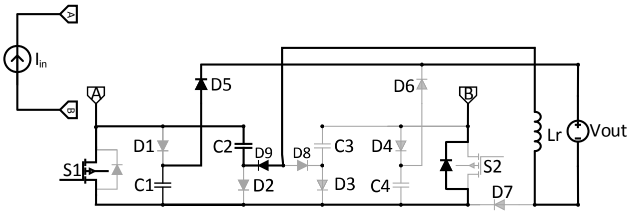
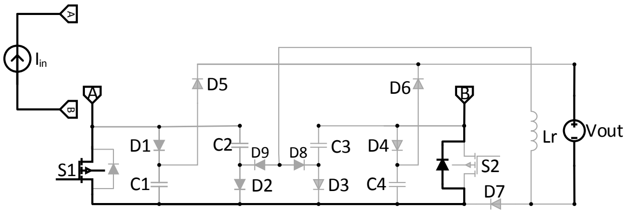


STAGE 3



STAGE 4

Figure 3. The equivalent circuits

B. Mode 2 ($t_1 < t < t_2$)

After the voltage of C_1 and C_2 reach to V_O, the diodes D_5 and D_7 turn on under ZVS condition. Thus, the voltage of C_1 and C_2 remains constant and the L_1 current is discharged to the output. In this mode the operation of converter is like the discharging mode in conventional boost converter. This mode last until S_1 is turned on by controller.

C. Mode 3 ($t_2 < t < t_3$)

At t_2 the switch S_1 is turned on and the diodes D_1 and D_2 are turned off. So a resonance occurs between C_1, C_2 and L_r. thus the voltage of C_1 and C_2 are reduced to reach zero and diode D_7 turned off under ZVS. The equations of this mode are:

$$\omega = \sqrt{\frac{2}{L_S . C_S}} \tag{3}$$

$$Z = \sqrt{\frac{2L_S}{C_S}} \tag{4}$$

$$i_{L2} = \frac{V_O}{Z} \sin \omega (t - t_2) \tag{5}$$

$$V_{C1} = V_{C2} = \frac{V_O}{2}\left[1 + \cos\omega\,(t - t_2)\right] \tag{6}$$

D. Mode 4 ($t_3 < t < t_4$)

At t_3 the voltages of capacitors C_1 and C_2 are equal to zero and also the current of inductor L_r becomes zero. Diode D_5 turns off under ZCS condition. Therefore input inductor is charged by input voltage like charging mode in conventional boost converter. Therefore the duration of this mode can be calculated by (7)

$$t_3 = \frac{\pi}{\omega} + t_2 \tag{7}$$

III. DESIGN STEPS

The proposed converter Consists of a bridgeless boost PFC converter and a lossless passive snubber. The design procedure of boost converter is similar to the conventional boost PFC converter. In the following the design procedure of proposed snubber circuit is given in two steps:

1. The snubber capacitors can be calculated like a conventional snubber capacitors therefore:

$$C_1 + C_2 \geq \frac{I_{in}.t_f}{0.2\,V_O} \tag{8}$$

2. The snubber inductor can be calculated from following equation:

$$L_r = \frac{{t_r}^2}{\pi.C_S} \tag{9}$$

It must be noted that: t_f is the switch fall time and t_r is the switch rise time.

IV. SIMULATION RESULTS

Based on previous section the proposed converter is design for $V_{in(ac)} = 140V_{RMS}$, $V_{out} = 340V_{DC}$ and P_{out}=290W. Therefore the circuit elements are L_1 = 500uH, $C_{1\sim4}$ = 2nF, L_r = 20uH, C_5 = 1000uF and R_1 = 400Ω. The proposed converter with the above value is simulated by PSIM and the simulation results are presented in Fig.5 and Fig.6.

Fig. 6(a) shows switching waveform of main switch. It can be seen from this figure, the switch S_1 is turned off under ZVS condition. The switching waveform of diode D_1 is shown in Fig. 6(b). This diode turns on under ZVS condition. Diode D_2 turns off under ZCS condition and turns on under ZVS condition as shown in Fig. 6(c).

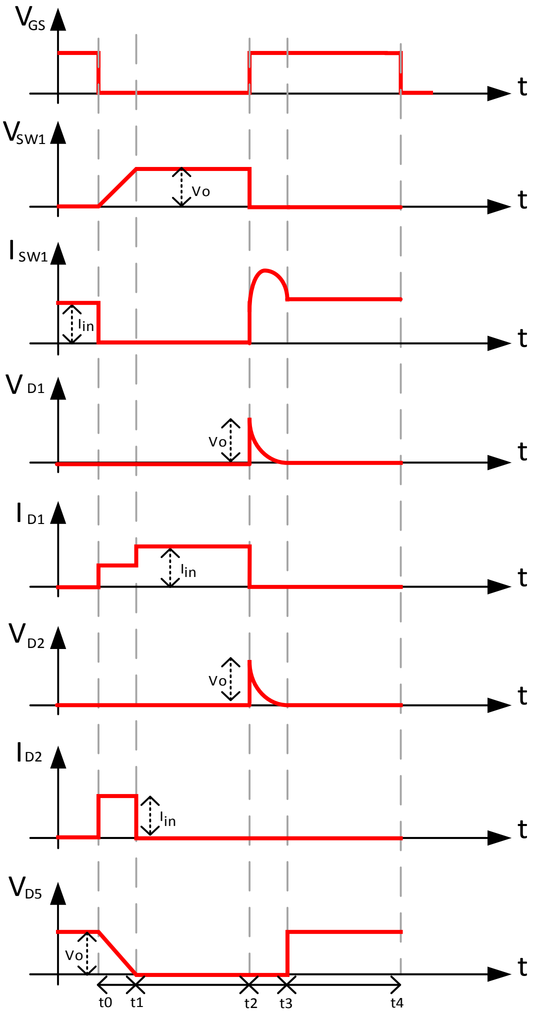


Figure 4. Theoretical Waveforms

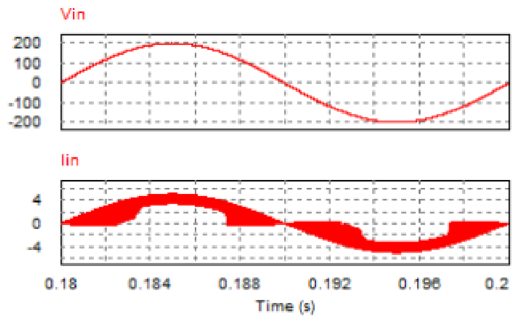
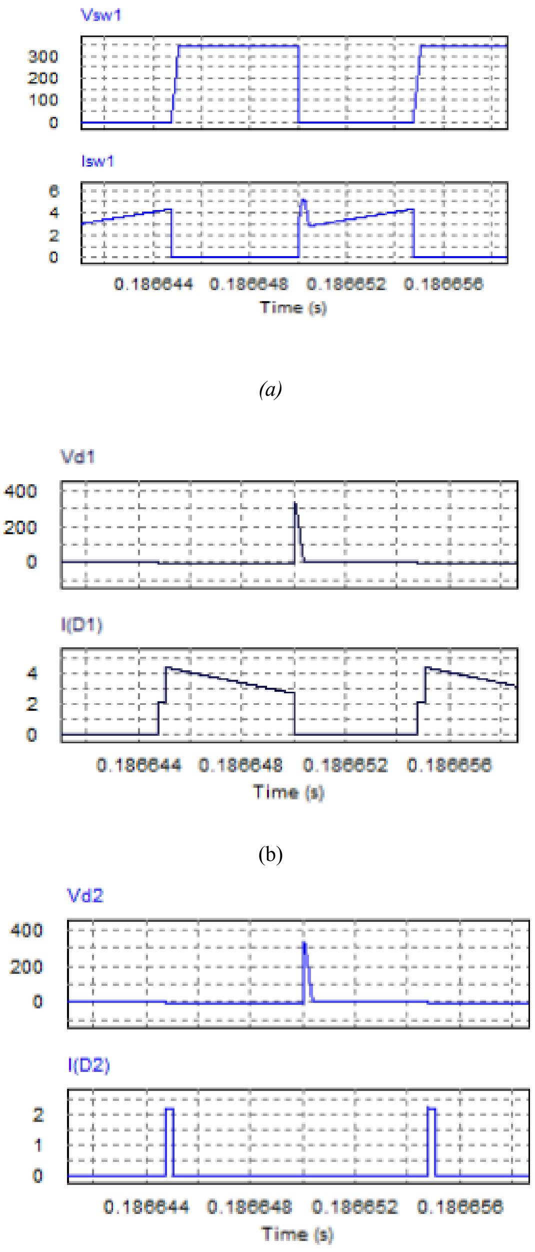


Figure 5. Input voltage and current waveforms

Fig. 7 shows the efficiency comparison between conventional boost converter with RCD snubber and purpose converter. As shown in Fig. 7, the proposed converter improve the efficiency by 5% at nominal load.

V. CONCLUSION

Increasing the switching frequency causes improving the power conversion density in the power electronic converters, increasing the switching losses and reducing the converter efficiency. The switching and conduction losses are two sources of losses in the switching converter. Thus to improve the efficiency, a new bridgeless soft switching PFC converter with a lossless snubber is introduced in this paper. The proposed converter is analyzed theoretically and the design consideration are given. As it was shown the soft switching condition is provided for all semiconductor elements. Finally the efficiency comparison was done by ORCAD software and it shows the proposed converter improves the efficiency about 5% at the nominal load.



(a)

(b)

(c)

Figure 6. The simulation Waveforms *a)* V_{S1} *and* I_{S1} *b)* V_{D1} *and* I_{D1} *c)* V_{D2} *and* I_{D2}

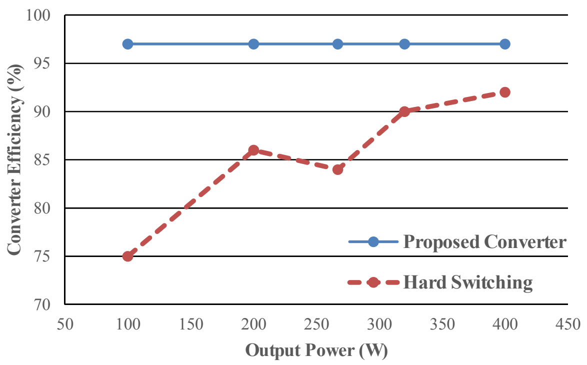


Figure 7. Efficiency diagram

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