A New High Efficiency High Power Factor ZVT Bridgeless PFC Converter

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Abstract – **In this paper, a new zero voltage transition (ZVT) bridgeless PFC converter with high power factor and high efficiency is presented. The proposed converter has not any extra voltage stresses on semiconductor elements. Main switches of the converter are switched under zero voltage (ZV) condition. Also the auxiliary switch is turned on under zero current (ZC) and turned off under zero voltage and current (ZVZC) condition. Due to use of bridgeless topology and soft switching technique simultaneously the converter's efficiency is higher than conventional counterpart. Also the proposed converter does not need the float gate driver. The operation of proposed converter is analyzed theoretically and the operation modes are presented. The design considerations are explained by a design example. The proposed converter is simulated by PSIM software to show the validity of theoretical analysis. The simulation results are compared with theoretical waveforms. The efficiency of simulation in ORCAD software shows 2% improvement in comparison with conventional PFC boost converter.**

Keywords- Boost converter, Bridgeless PFC converter, Conduction losses, Switching losses, Zero voltage transition (ZVT).

I. INTRODUCTION

Nowadays, 3rd, 5th and 7th harmonics pollution is one of the most important problems in power networks. These harmonics are increased because of the nonlinear loads connection to the power networks. Input rectifier of electronic devices is important and used widely in nonlinear loads. These harmonics cause some problems such as heating transformers, increasing parallel capacitors current, deterioration of the voltage waveform and etc [1]. To solve the above mentioned problems, the power factor correction (PFC) converters are used in the input of rectifiers. Therefore, the conduction losses are increased in comparison with conventional rectifier because; in the PFC converters a boost converter is used after the input rectifier [2]. In this literature, various methods for reducing conduction losses such as bridgeless PFC converters, single-stage PFC converters are presented [3]-[4]. The advantage of using bridgeless PFC in converters is the application of these converters in the devices that requires a dc link. For further increasing of the efficiency, soft switching techniques such as zero current transition (ZCT), zero voltage transition(ZVT) and zero current zero voltage transition (ZCZVT) are used [5]-[6]. So by reducing conduction losses due to the using bridgeless PFC in converter and reduce switching losses due to the using soft switching techniques, it is possible to achieve maximum efficiency [7]. To reduce the size and weight of converter, the switching frequency must be increased, so the use of the MOSFET switches are inevitable. Because of the turn on MOSFET capacitive losses problem, ZV soft switching techniques are used. The ZVT bridgeless PFC converters that were presented in previously published papers have some problems. In [8], the auxiliary switch turning off is hard. A floating gate driver is needed for the auxiliary switch in [9]. The voltage and current stresses on auxiliary circuit are high in [10]. In [11] C_{s1} is used to provide ZVS condition for turning off S_1 instantly. It causes increasing the conduction losses.

In this paper a new ZVT bridgeless PFC converter is proposed to solve mentioned problems. In comparison with [11] the using of C_{b1} and C_{b2} in the proposed converter causes that this energy discharge completely into the output and thus the effective switch current and conduction losses are decreased. Furthermore the complexity of driver is reduced because it does not need to float gate driver. The voltage stresses in the auxiliary circuit are low. In the next section, the proposed converter is introduced and theoretical analysis is presented. Section III presents design considerations and controller block diagram of the converter. The section IV presents the simulation of proposed converter by designed elements in section III. These results are compared with theoretical analysis and the accuracy of the theoretical analysis is examined.

II. PROPOSING PFC CONVERTER AND THEORETICAL DESCRIPTION

The proposed bridgeless PFC converter is shown in Fig. 1. The auxiliary circuit elements of proposed converter are shown in the dotted box. The other elements include a bridgeless PFC converter which consists of the two boost converter for two half line cycle. The auxiliary circuit provides soft switching condition for all of the semiconductor elements. The operation of proposed converter in both half line cycles is similar. Therefore, the proposed converter is analyzed in one switching cycle in positive half line. Assuming the proposed converter operates in steady state and continuous conduction mode (CCM). Also the input current and output voltage ripple in a switching cycle is ignored. Thus input inductor and output capacitor considered as ideal DC current and voltage source respectively in a switching cycle. Also for theoretical analysis all of the elements considered

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as ideal. The converter in a switching cycle has eight modes. Before the first mode all semiconductor elements except D_1 and body diode of S_2 are off. So the converter operation is like transmitting energy to the output in the conventional boost converter. Also initial voltage of capacitors C_{s1} and C_{b2} are Vo and initial voltage of capacitor C_{b1} is zero.

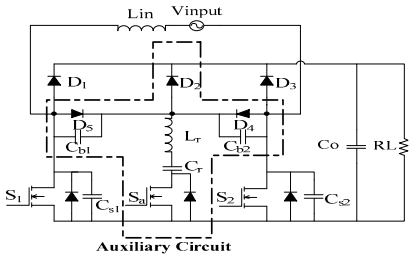


Figure 1. proposed ZVT bridgeless PFC converter

Mode 1 [t0<t<t1] (Fig. 3(a)):

This mode starts with turning on S_a under zero current switching (ZCS) condition. When S_a is turned on a resonance occurs between C_r and L_r. At the end of this mode, the resonant current (I_{Lr}) will increased to reaches the input current (I_{in}). Therefore in this time the D_1 current reaches zero and it turns off under ZVZCS condition. The resonant inductor current I_{Lr} and resonant capacitor voltage V_{cr} are presented as following:

$$I_{Lr} = (V_o - V_{Cr0}).\sin(\omega_{r1}.t) \quad (1)$$

$$V_{Cr} = (V_{Cr0} - V_o).\cos(\omega_{r1}.t) \quad (2)$$

Where V_{Cr0} is initial capacitor voltage before the first mode and $\omega_{r1} = \frac{1}{\sqrt{L_r.C_r}}$

Mode 2 [t1<t<t2](Fig. 3(b)):

In this mode C_{s1} and C_{b2} begin to discharge in the auxiliary circuit. The I_{Lr} continues to increase. When C_{s1} and C_{b2} are fully discharged, this mode is finished. Equations in this mode thus presented:

$$I_{Lr} = A.\cos(\omega_{r2}.t) + B.\sin(\omega_{r2}.t) + I_{Lr}.\frac{C_{r2}}{C_{p2}} \quad (3)$$

$$V_{cs1} = (\frac{B}{C_{s1}}.\cos(\omega_{r2}.t) - \frac{A}{C_r}.\sin(\omega_{r2}.t) + I_{Lr1}.\frac{C_{s1}-C_r}{C_{s1}^2}.t + V_o - \frac{B}{C_{s1}} \quad (4)$$

Where $C_{p2} = C_{s1} + C_{b2}$, $C_{r2} = \frac{C_{p2}.C_r}{C_{p2}+C_r}$, $\omega_{r1} = \frac{1}{\sqrt{L_r.C_{r2}}}$, $A = I_{in}.\frac{C_{r2}}{C_r}$, $B = \frac{V_o - V_{Cr1}}{\omega_{r2}.L_r}$, $I_{Lr1}=I_{Lr}(t_1)$ and $V_{Cr1}=V_{Cr}(t_1)$

Mode 3 [t2<t<t3](Fig. 3(c)):

This mode is started by turning on D_4 and body diode of S_1. Therefore S_1 can be turned on under zero voltage zero current switching (ZVZCS) condition. Thus inductor current decreases until it reaches I_{in}. Equations in this mode are presented:

$$I_{Lr} = I_{Lr2}.\cos(\omega_{r3}.t) - \frac{V_{cr2}}{\omega_{r3}.L_r}.\sin(\omega_{r3}.t) \quad (5)$$

Where $\omega_{r3} = \frac{1}{\sqrt{L_r.C_r}}$, $I_{Lr2}=I_{Lr}(t_2)$ and $V_{Cr2}=V_{Cr}(t_2)$

Mode 4 [t3<t<t4](Fig. 3(d)):

Decreasing of the L_r current continues until it reaches I_{in}. Therefore in this mode I_{in}-I_{Lr} flow through S_1. This mode last until L_r current reaches zero value. Equations in this mode are presented as following:

$$I_{Lr} = I_{Lr3}.\cos(\omega_{r4}.t) - \frac{V_{cr3}}{\omega_{r4}.L_r}.\sin(\omega_{r4}.t) \quad (6)$$

Where $\omega_{r4} = \frac{1}{\sqrt{L_r.C_r}}$, $I_{Lr3}=I_{Lr}(t_3)$ and $V_{Cr3}=V_{Cr}(t_3)$

Mode 5 [t4<t<t5](Fig. 3(e)):

In this mode I_{Lr} is reversed and the body diode of S_a is turned on. Therefore S_a can be turned off at ZVZCS condition. In this mode D_4, D_5 are turned off and C_{b1}, C_{b2} starts to charge to reach the output voltage to (V_o). When it reaches V_o, D_2 is turned on and clamp the voltage at V_o. This mode is finished by discharging of the L_r completely. In this mode the following equations are obtained:

$$I_{Lr} = -(C_{r5}.\omega_{r5}.V_{cr4}.\sin(\omega_{r5}.t)) \quad (7)$$

Where $C_{p5} = C_{b1} + C_{b2}$, $C_{r5} = \frac{C_{p5}.C_r}{C_{p5}+C_r}$, $\omega_{r5} = \frac{1}{\sqrt{L_r.C_{r5}}}$, $I_{Lr4}=I_{Lr}(t_4)$, $V_{Cr4}=V_{Cr}(t_4)$

Mode 6 [t5<t<t6] (Fig. 3(f)):

In this mode S_1 current is equal to I_{in}, and converter operates like a conventional boost converter. The input inductor (L_{in}) is charged linearly. The duration of this mode is determined by the controller.

Mode 7 [t6<t<t7] (Fig. 3(g)):

This mode is started by turning off S_1 under zero voltage switching (ZVS) condition. In this time, C_{s1} and C_{b1} are charged and discharged respectively and transmit energy through the D_2 at the output. This mode is finished by reaching V_{cs1} at the output voltage and C_{b1} completely discharging. In this mode V_{cs1} is:

$$V_{cs1} = \frac{I_{in}}{C_{r7}}.t \quad (8)$$

Where $C_{r7} = C_{b1} + C_{s1}$

Mode 8: [t7<t<t8] (Fig. 3(h)):

D_2 is turned off and D_1 is turned on when C_{b1} is completely discharged, this mode is like power transfer to the output in the conventional boost converter. This mode last until next switching cycle.

III. DESIGN CONSIDERATIONS

The design considerations are presented in four sections and are given as following:

1- Auxiliary circuit elements (L_r, C_r):.

Resonant inductor must be large enough to reduce di/dt of the switch and diode. In the other hand, if the value is selected too high, the conduction losses are increased. So the above requirements must be considered to select resonant inductor. By selecting the turning off duration of the D_1 six times greater than t_{rr}, following equation is obtained to calculate L_r.

$$L_r = \frac{6*t_{rr}*V_{peak\_sa}}{I_{in}} = \frac{6*60ns*(0.7*380)}{2} = 4.8\ \mu H \quad (9)$$

To provide soft switching condition for semiconductor elements, C_{b1},C_{b2} and C_r are calculated (by assuming Z_r=15Ω, K=6)

$$C_r = \frac{L_r}{(Z_r)^2} = \frac{4.8\ \mu H}{(15)^2} = 21.3\ nF \qquad (10)$$

$$C_{b1} = C_{b2} = \frac{C_r}{K} = \frac{21.3\ nF}{6} = 3.55\ nF \qquad (11)$$

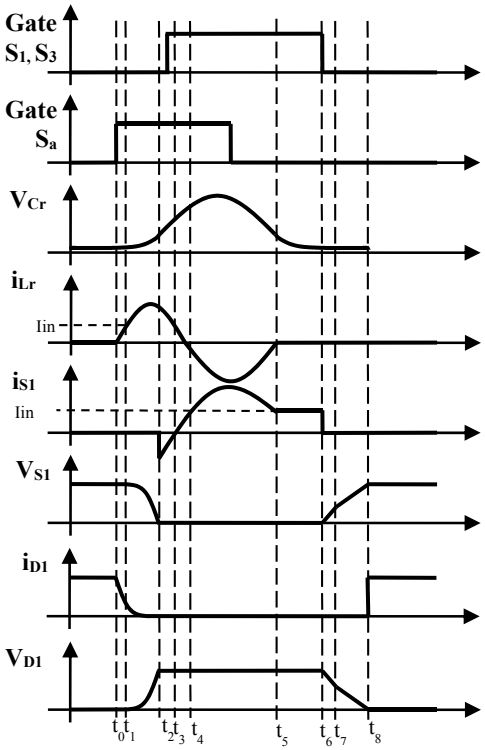


Figure 2. Theoretical waveform of proposed bridgeless PFC converter.

2- Selection of switches:

The peak voltage on the all switches is equal to:

$$V_{s1,s2,sa\ max} = V_{o\ max} \qquad (12)$$

Also the peak current that through on the switches is presented as the following:

$$I_{s1,2\ max} = I_{in\ max} + \Delta I_{Lin}/2 \qquad (13)$$

$$I_{sa\ max} = \frac{Vo}{Z_{r2}} \qquad (14)$$

Where $Z_{r2} = \sqrt{\frac{L_r}{C_{r2}}}$

3- Selection of diodes:

The peak voltage and current of diodes are presented as the following:

$$V_{D1,D2,D3\ max} = V_{o\ max} \qquad (15)$$

$$I_{D1,D3\ max} = I_{in\ max} \qquad (16)$$

4- Control circuit:

The controller of proposed PFC rectifier is similar to conventional PFC rectifier except two monostable and one XOR gate. These elements can be added to any conventional controller to provide auxiliary switch gate signal. The block diagram of controller is shown in Fig. 4. For simplicity, the peak current control is used.

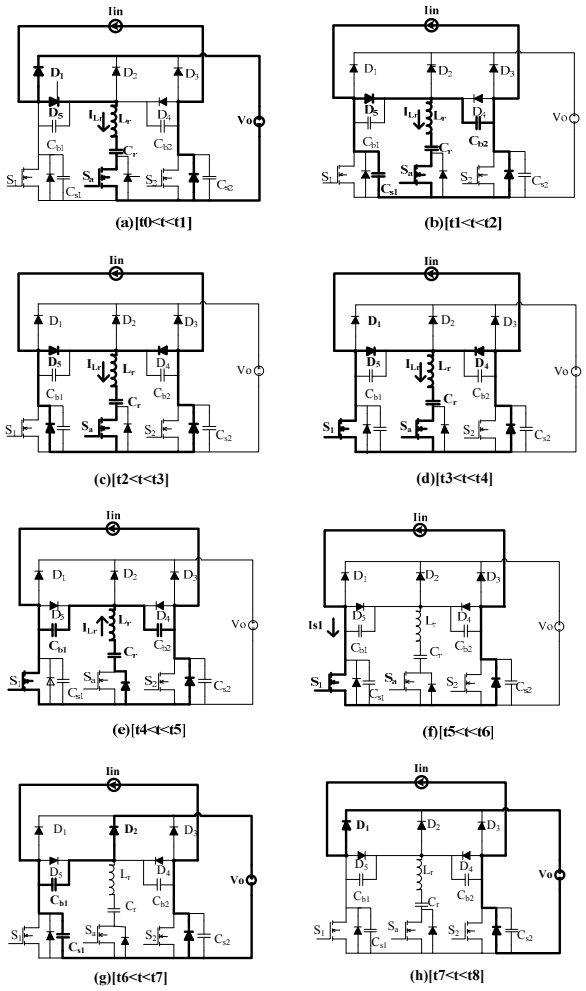


Figure 3. The equivalent circuit models.

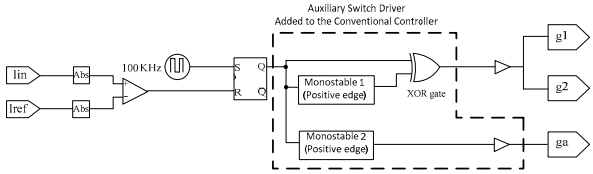
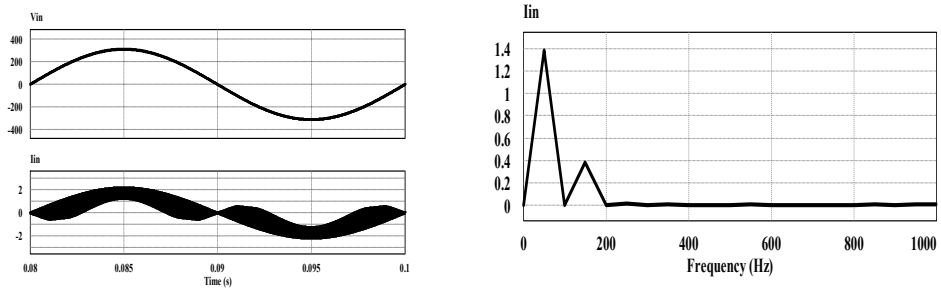


Figure 4. Block diagram of Control circuit

IV. .SIMULATION RESULTS

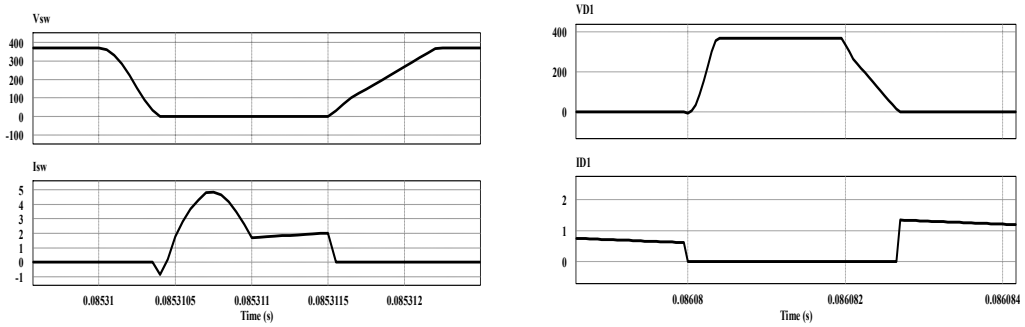
Based on previous section the proposed converter is designed for V_{in}= 310 v_{rms}, V_o= 380 v_{dc}, P_o= 200 W and $F_{switching}$= 100 kHz. According to the design considerations, the circuit element values are Lr= 5 µH, C_r= 22.5 nF, C_{b1}=C_{b2}= 3.5 nF, Lin= 500 µH, C_o= 1000 µF. In this section, the converter is simulated by Power Simulator (PSIM) software. Fig. 5(a) shows the input current and voltage simultaneously. This shows that the input current and voltage are in phase and the average of input current is sinusoidal. The harmonics of input current is shown in Fig. 5(b). It can be seen from this figure that this converter can easily satisfy the IEC-61000-3-2 electromagnetic compatibility standard. Fig. 6(a) and (b) show the current and voltage waveforms of the main switch (S_1) and main diode (D_1) respectively. Fig. 6(a) shows the main switch is turned on under ZVZC condition and turned off under ZV condition. The main diode turns off under ZVZC condition and turns on under ZV condition as it is shown in Fig. 6(b). All

of the simulation results that are presented in this section confirm the theoretical analysis. For the efficiency comparison between proposed converter and conventional bridgeless boost PFC circuit, the proposed converter and conventional one are simulated in OrCAD software. The measured efficiency in different output power is shown in Fig. 7. The proposed converter improved the efficiency in nominal output power by 2%.



(a) (b)

Figure 5. (a) Input Voltage and Current waveform, (b) Input current harmonic.



(a) (b)

Figure 6. (a)Voltage and Current waveform of main switch, (b) voltage and current waveform of main diode.

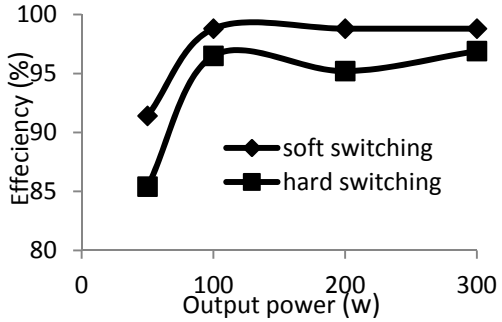


Figure 7. Efficiency comparison.

V. CONCLUSIONS

In this paper a bridgeless ZVT PFC converter proposed and analyzed. In comparison to other soft switching PFC converters, the proposed PFC converter has advantages such as using fewer elements, providing soft switching conditions for all switches. Furthermore conduction losses in this converter are low, due to completely discharge of the C_{b1} capacitor in the output and using bridgeless topology. Also due to providing soft switching condition for all semiconductor elements, the switching losses are reduced. The proposed converter is analyzed. The simulation results confirm the theoretical analysis. The design procedure with a design example was presented. The simulation shows 2% improvement in comparison with conventional one. Also the input current is sinusoidal and the power factor is near unity.

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