

# Time Domain CCM/DCM Boundary Detector with Zero Static Power Consumption for Integrated High-Efficiency Step-down DC/DC Converters

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**Abstract**—this paper describes a circuit allowing accurate detection of the continuous (CCM) and discontinuous (DCM) conduction mode boundary. It is suitable namely for very low power integrated DC/DC converters such as the buck or boost. The zero power consumption of this critical block enables to greatly improve the light load power efficiency, and minimize the silicon area. Detection uses a time shift of the power-stage output voltage, which depends on the inductor current value and its polarity. Detector circuit is realized with a digital latch comparator containing only a few digital gates. The paper contains description of the method, example of circuit implementation, and post-layout simulation of integrated detector in 0.13 $\mu\text{m}$  CMOS technology, allowing to obtain several mA detection accuracy.

**Keywords**—CCM/DCM boundary detection, pulse-skipping, DC/DC converter low-power mode, zero valley current detection, synchronous rectifier.

## I. INTRODUCTION

Typical switched-mode DC/DC converter such as buck (step-down) or boost (step-up) handle a wide range of load current  $I_{\text{LOAD}}$ . Compared to linear regulators (LDO), switches mode converters offer high power efficiency in a wide output current range. The efficiency  $\eta$  is mainly determined by the power loss  $P_{\text{LOSS}}$ , being typically expressed as a sum of ohmic and dynamic contributions  $R \cdot I^2$  and  $CV^2 f_{\text{SW}}$  [1, 2]:

$$P_{\text{LOSS}} = R \cdot I_L^2 + CV_{\text{DD}}^2 f_{\text{SW}}$$

In this equation,  $R$  corresponds to an average resistance in the inductor current path, and  $C$  to the sum of capacitors periodically charged-discharged to the power supply voltage  $V_{\text{DD}}$  with switching frequency  $f_{\text{SW}}$  [2]. Typically, power loss at high current is dominated by the ohmic power  $R \cdot I^2$ , whereas power loss at light load is dominated by the constant dynamic (switching) power  $CV^2 f_{\text{SW}}$ .

In order to decrease the dissipated power  $P_{\text{LOSS}}$ , power efficiency  $\eta$  for high output current is improved by the low  $R_{\text{ON}}$  and  $ESR$  of the power transistors and inductor, respectively. The middle output power efficiency can be optimized *e.g.* by the dynamic adjusting of the segmented power stage size such as [2] or [3]. At light load operation, low power modes such as pulse-skipping (PSK), pulse-frequency modulation (PFM) or burst-mode are used [1], [4]. These modes also avoid CCM operation with negative inductor current  $I_L < 0$ .

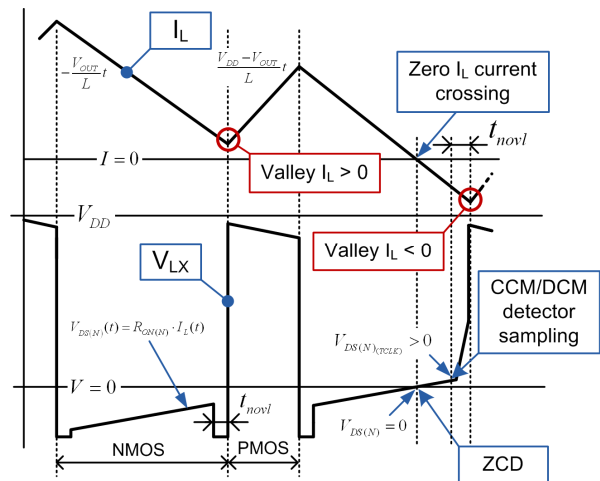


Fig. 1. Details of inductor current  $I_L$  and output voltage  $V_{\text{LX}}$  of the buck-converter power stage shown in Fig. 2 [5].

Consequently, transition between CCM/DCM is defined by the *zero valley inductor current*  $I_{L(\text{VALLEY})}$  [1]. An example of the transition between positive and negative  $I_{L(\text{VALLEY})}$  is shown in Fig. 1.

Due to the inductor current ripple  $\Delta I_L$  depending on inductor value  $L$ , power-supply voltage  $V_{\text{DD}}$ , output (1) voltage  $V_{\text{OUT}}$ , and switching frequency  $f_{\text{SW}}$ , the zero valley-current is difficult to predict from the operating point of the DC/DC converter. Therefore, circuits allowing measure the polarity of the inductor-current was developed in the past. These circuits can be divided in two categories [5]:

a) **Zero current crossing detectors (ZCD):** provide fast (immediate) information, that inductor current crosses the zero value during the NMOS conduction phase. This detector allows to realize synchronous rectification [6].

b) **Negative  $I_L$  valley current detectors:** measure (sample) the inductor current polarity at the end of NMOS conduction cycle and provide the information afterwards (circuit labeled here as CCM/DCM boundary detector). These circuits do not require fast detection [8].

Typically, circuits for ZCD or CCM/DCM boundary detection measure the polarity of the power mosfet drain-

source voltage  $V_{DS} = I_L \cdot R_{DS(on)}$ . However low on-resistance  $R_{DS(on)}$  along with nearly zero  $I_{L(VALLEY)}$  yield very low (several millivolts) useful voltages  $V_{DS}$ . Consequently detection of this very low voltage requires accurate and (in case of ZCD) fast comparator, which presents the most sensitive element of the DC/DC converters [5].

This paper presents CCM/DCM boundary detector initially presented in [7], and based on the time property of the output switching voltage  $V_{LX}$ . This allows to provide detection insensitive to  $R_{DS(on)}$ . The detector is described in section II. Section III describes the implementation in CMOS, whereas the post-layout simulations of the detector are shown in section IV.

## II. TIME DOMAIN CCM/DCM BOUNDARY DETECTOR

The operation of the detector is described on example of the buck converter power stage shown in Fig. 2. This power stage contains an input PWM signal CMD\_MOS, a dead time generator (anti shoot-through circuit), power transistors, and output LC filter.

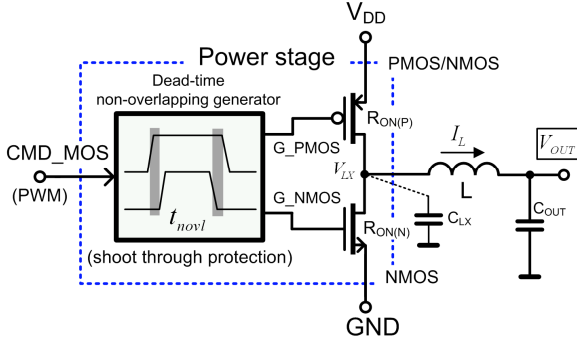


Fig. 2. Step-down converter power stage with output LC filter [5].

As shown in Fig. 1, switching cycle of  $V_{LX}$  voltage consists of:

- 1) *NMOS conduction*, where  $V_{LX}$  is low and present small decrease due to the triangular inductor current ripple,
- 2) *non-overlapping* (high output impedance) phase, where both transistors are off and the PMOS or NMOS transistor substrate diodes can enter in conduction.
- 3) *PMOS (high-side transistor) conduction*, where  $V_{LX}$  is close to  $V_{DD}$  and decrease with time due to the triangular inductor current ripple.

As shown in Fig. 1, the minimum (valley) inductor current appears during the transition between NMOS and PMOS conduction. This transition is shown in detail by idealized simulation in Fig. 3. This figure shows the non-overlapping gate voltages  $G_{NMOS}$ ,  $G_{PMOS}$ , and also the transition of  $V_{LX}$  for three values of  $I_{L(VALLEY)}$ .

The transition between NMOS  $\rightarrow$  PMOS conduction starts with opening the bottom NMOS switch. The power stage enters into high impedance, and  $V_{LX}$  is maintained by the parasitic capacitance  $C_{LX}$ . Upon the polarity of the valley inductor current, the parasitic capacitor  $C_{LX}$  is *i*) charged to negative voltage if  $I_L > 0$ , *ii*) remain unchanged for  $I_L = 0$ , or *iii*) is charging to positive voltage if inductor current is negative.

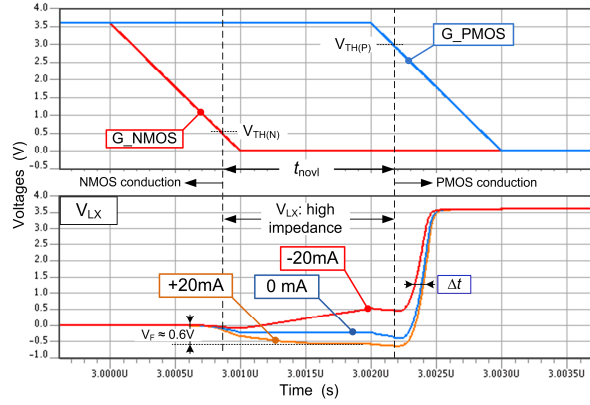


Fig. 3. Idealized  $V_{LX}$  voltage GND  $\rightarrow$   $V_{DD}$  transition during the non-overlapping phase as function of the value  $I_{L(VALLEY)}$ .

The voltage change  $\Delta V_{LX}$  accumulated during  $t_{novl}$  creates a time delay  $\Delta t$  at the opening of the high-side PMOS transistor. This delay is used for the valley current polarity detection.

### A. Analysis of $V_{LX}$ Voltage transition from GND to $V_{DD}$

As previously mentioned,  $V_{LX}$  voltage have different behavior depending on the polarity of  $I_{L(VALLEY)}$  during the non-overlapping phase (*i.e.* when  $I_{L(VALLEY)}$  the power stage is at high impedance).

The unwanted (DCM) scenario with  $I_L < 0$  (inductor current enters into  $V_{LX}$  node) results in  $C_{LX}$  being charged to positive voltage. As shown in previous Fig. 3 and detailed in Fig. 4,  $V_{LX}$  increases with positive *slope*<sub>1</sub>. Compared to this, zero value of  $I_{L(VALLEY)}$  keeps  $V_{LX}$  constant. Positive  $I_{L(VALLEY)} > 0$  (required in CCM), charge  $C_{LX}$  to negative voltage up to the opening of NMOS substrate diode ( $V_F \approx -0.6V$ ).

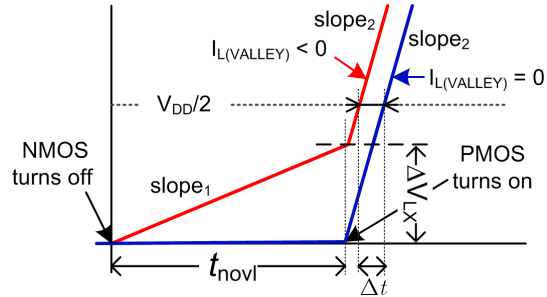


Fig. 4. Demonstration of time shift of  $V_{LX}$  voltages for zero and negative  $I_L$ .

The value of *slope*<sub>1</sub> can be estimated from  $I_{L(VALLEY)}$ , and parasitic capacitance  $C_{LX}$ . This capacitance is approximately given by the overlap and drain junction capacitances:

$$C_{LX} = C_{OX}L_D(W_P + W_L) + C_j(W_P + W_L) \quad (2)$$

where  $C_{OX}$  is oxide capacitance per unit area,  $L_D$  drain overlap (lateral diffusion) length, and  $C_j$  total junction capacitance. For example,  $C_{LX}$  reach  $\sim 100pF$  for 1A power stage, and is therefore dominant compared to other (bounding or PCB) capacitances. *Slope*<sub>1</sub> can be then expressed as:

$$slope_1 = \frac{\Delta V_{LX}}{\Delta t} = \frac{I_{L(VALLEY)}}{C_{LX}} \quad (3)$$

At the beginning of PMOS conduction phase,  $V_{LX}$  voltage starts immediately raise with very high  $slope_2$ . We can see that  $slope_2 \gg slope_1$  (Fig. 3-5). Due to this very high slew-rate, it is difficult to determine its exact value. However, we can consider that  $slope_2$  is independent on  $I_{L(VALLEY)}$ . This assumption has been verified by measurements shown in Fig. 5, provided on integrated 0.13 $\mu$ m CMOS 1000mA buck converter.

Due to the positive offset  $\Delta V_{LX}$  created during the non-overlapping phase with negative (unwanted) valley current  $I_L$  Fig. 4,  $V_{LX}$  voltage has small time advance compared to the zero-current (reference) characteristic. This voltage shift  $\Delta V_{LX}$  can be expressed as:

$$\Delta V_{LX} = \frac{I_{L(VALLEY)} \cdot t_{novl}}{C_{LX}} \quad (4)$$

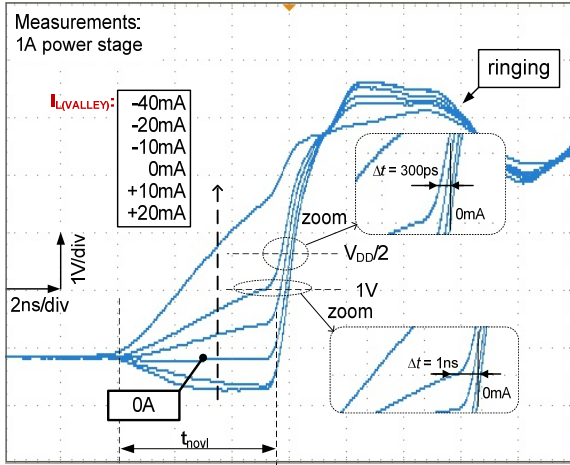


Fig. 5. Measured  $V_{LX}$  voltage transition during the non-overlapping phase as function of the valley inductor current  $I_{L(VALLEY)}$  [7].

The time advance  $\Delta t$  can be expressed as a function of  $slope_2$ :

$$\Delta t = \frac{\Delta V_{LX}}{slope_2} = \frac{I_{L(VALLEY)} \cdot t_{novl}}{C_{LX} \cdot slope_2} \quad (5)$$

The time delay  $\Delta t$  is in order of hundredth of picoseconds and can be detected by a digital circuit described in the following.

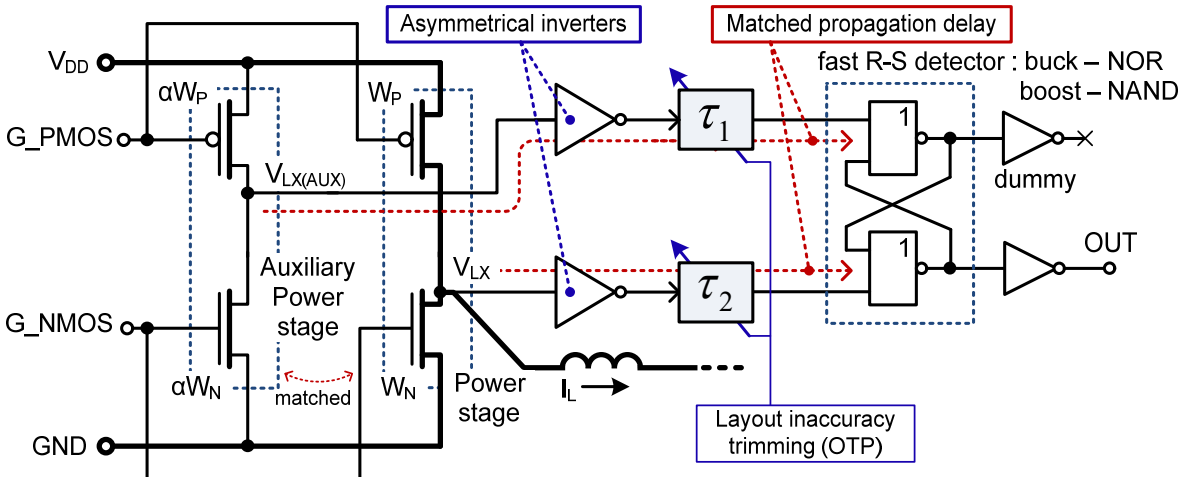


Fig. 6. CCM/DCM boundary detector with buck converter power stage. Variant for boost converter use NAND gates in R-S latch comparator.

### III. IMPLEMENTATION OF DETECTION CIRCUIT

The time domain CCM/DCM boundary detector [7] used for step-down DC/DC converter is shown in Fig. 6. This circuit includes main power stage, auxiliary (very small) reference power stage, blocks of programmable delay, asymmetrical inverters, and digital (latch) R-S comparator.

In order to realize the detection of  $\Delta t$ , reference signal  $V_{LX(AUX)}$  should be created. While the main power stage delivers output current  $I_L$ , the auxiliary power stage is open-ended and provide  $I_{OUT} = 0$ . The behavior of  $V_{LX(AUX)}$  corresponds to  $V_{LX}$  for  $I_{L(VALLEY)} \approx 0$ . This provide a required reference signal for the digital latch R-S comparator.

#### A. Digital R-S Comparator

The R-S digital (latch) comparator [9] operates as follow: during NMOS condition, both  $V_{LX}$  and  $V_{LX(AUX)}$  are at *low* ( $\sim GND$ ). R-S flip-flop is in forbidden (undefined) state, and the output OUT is *high*. During  $t_{novl}$ ,  $V_{LX}$  evolve upon polarity of  $I_{L(VALLEY)}$ , whereas  $V_{LX(AUX)}$  remain unchanged ( $\sim 0V$ ). Switch-on event of the PMOS transistor make simultaneously rise  $V_{LX}$  and  $V_{LX(AUX)}$  with identical  $slope_2$ . If  $V_{LX}$  reach comparator threshold *before*  $V_{LX(AUX)}$ , output OUT switches to *low*. This signify, that  $I_{L(VALLEY)} < 0$ , and DC/DC converter is preferably to be used in low-frequency (pulse skipping) mode. On the contrary, when  $V_{LX}$  reach comparator threshold *after*  $V_{LX(AUX)}$ , output OUT remain high during whole PMOS conduction. This signify that  $I_{L(VALLEY)} > 0$ , what is advantageous for maintaining CCM.

As shown in Fig. 5, time delay  $\Delta t$  is very small. Its detection is therefore difficult. More specifically,  $\Delta t$  reach roughly several hundreds of picoseconds. Accurate handling of such very fast signals requires very good matching of  $V_{LX}$  and  $V_{LX(AUX)}$  signal paths. However, this is difficult in practice, namely due to usually very large power transistors. On this account, programmable delays  $\tau_1$  and  $\tau_2$  of approximately 0 to 1ns were added. These delays allow to compensate the layout mismatch, and also to adjust (calibrate) the detector accuracy. Moreover these delays help to avoid a negative  $\Delta t$  for  $I_{L(VALLEY)} = 0$ , which can render impossible the detection. Variable delays are made of programmable cascaded inverters, and it is assumed, that one particular calibration will be valid for all realized converters.

## B. Assymetrical Inverters

Generally, CMOS logic cells provide switching point approximately  $V_{DD}/2$ . However, as shown in measured characteristic Fig. 5, decrease of the switching point voltage can be advantageous. This allows to increase the time delay  $\Delta t$ , and thus increase the reliability of detection. Lowering the switching point can be obtained by use asymmetrical inverters (skewed gates) [10]. This can be realized *e.g.* by enlarge NMOS transistor channel width  $W$  as:

$$\left(\mu_N \frac{W}{L}\right)_{NMOS} > \left(\mu_P \frac{W}{L}\right)_{PMOS} \quad (6)$$

where  $\mu_{N,P}$  are the electron/hole mobility. Employing this condition allows to reach the switching point close to  $V_{TH}$ . In order to provide switching point voltages equal for  $V_{LX}$  and  $V_{LX(AUX)}$ , both asymmetrical inverters from Fig. 6 should be matched.

## IV. SIMULATED RESULTS INTEGRATED CONVERTER

The step-down DC/DC converter designed for  $I_{OUT(max)} = 1A$  was layouted in 130nm 5V CMOS. The results obtained by the post-layout simulation allowed to verify the operations of the described detector in wide operating range. An example of the post-layout (extracted) simulated response is shown in Fig. 7. Here, DC/DC converter was operated in forced CCM, while the load current was linearly increasing. The detector generates output signals “low” for negative valley inductor current, as described in section III.

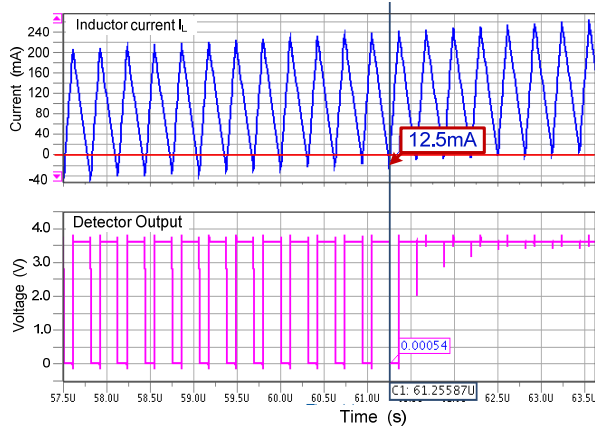


Fig. 7. Example of the detector output voltage for de-dc converter operated in CCM and linearly increasing load current.

TABLE I.

RESULT OF POST-LAYOUT SIMULATION OF 1AMPS CONVERTER LAYOUTED IN 0.13 $\mu$ m CMOS ( $L = 1\mu H$ ,  $f_{sw} = 3.2MHz$ ,  $\alpha = 0.0001$ ).

$V_{DD}$ (V)	$V_{REF}$ (V)	Temp ( $^{\circ}C$ )	$I_{TH}$ (mA)
3.6	0.6	-25	-11.5
2.5	0.6	-25	-6.5
4.8	0.6	-25	-20.6
3.6	1.8	-25	-14.6
2.5	1.8	-25	-9.0
4.8	1.8	-25	-19.0
3.6	0.6	125	-12.3
2.5	0.6	125	-6.1
4.8	0.6	125	-15.5
3.6	1.8	125	-12.3
2.5	1.8	125	-9.5

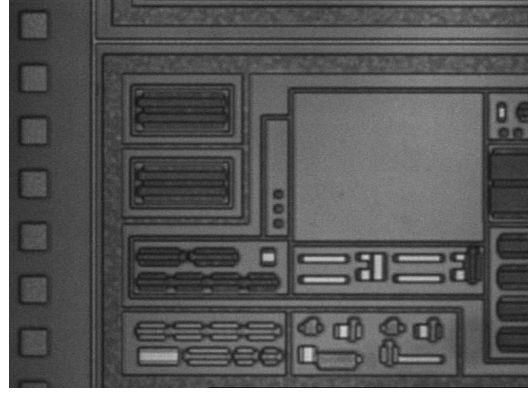


Fig. 8. Layout of the CCM/DCM detector in 0.13 $\mu$ m CMOS.

Tab. I shows values of the detection threshold  $I_{TH}$ . The accuracy of  $I_{TH}$  was verified in wide operation range, what allows to demonstrate the reliability of the detection method.

## CONCLUSION

Presented paper describes practical realization of the CCM/DCM boundary detector, exploiting the time-property of  $V_{LX}$  voltage. Thanks to the quasi-digital implementation, it achieves zero static power consumption, and require very small integration surface. This makes this detector a key element of the ultra-low power and high efficiency DC/DC converter. Future work aims the measurements of integrated detector and elaboration of reliable automatic mode selection (AMS) algorithm.

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