130 nm CMOS Fully Differential SC Filter for Ultra-Low Voltage Σ-Δ Converter

David Maljar, Daniel Arbet and Viera Stopjaková

Institute of Electronics and Photonics
Faculty of Electrical Engineering and Information Technology
Slovak University of Technology
Email: daniel.arbet@stuba.sk

***Abstract*—In this paper design and function of the fully differential (FD) switched-capacitor (SC) integrator for ultra-low voltage Sigma-Delta analog to digital converter (Σ-Δ ADC) are presented. The proposed integrator was designed for differential input signal and applicable as a main analog block of ultra-low voltage Σ-Δ ADC in standard 130 nm CMOS technology. The main block of proposed integrator is operational transconductance amplifier (OTA) based on two-stage Rail-to-Rail (RtR) FD operational amplifier (OPAMP) working in sub-threshold regime. The characteristic properties of this circuit is non-standard OTA topology, using SC common-mode feedback (CMFB) circuit and using switching T-gates. All of these subcircuits are supplied by only 0.6 V with achieved gain 24.09 dB and cutoff frequency 165.95 kHz.**

***Keywords*—analog design, ultra-low voltage, switched-capacitor integrator, Sigma-Delta ADC, CMOS**

I. Introduction

Nowadays, analog designers are facing difficult challenges due to evolution of CMOS nanometer technology and continuous scaling-down of the power supply voltage of integrated circuits (IC). These things cause decreasing dimensions of transistors and affect to the properties of the analog circuits. Usage of transistors as resistors, capacitors, amplifiers or current sources is still needed in analog design but the requirement to minimize the supply voltage brings many problems. For example, more than 2 or 3 transistors cannot be stacked because of the voltage headroom issue. In addition, many of them work in weak inversion region where current I_D exponentially depends on voltage V_{GS} and where is considerable parasitic capacitance effect. On the contrary, in digital design, transistors are mostly used as the switches and there are not so many problems of this kind with them. It is one of the most important advantage of digital ICs.

ADCs has been moved to the CMOS nanometer technologies as an interface between analog and digital circuits. Both of these kinds of circuits are implemented on single chip, so they have to be power-supplied by one V_{DD} voltage. Since the digital part of the circuit can operate with an ultra-low supply voltage, the analogue parts of the circuit are adapted to these ultra-low values of V_{DD} as much as possible. In $\Sigma - \Delta$ ADC is low-pass filter - integrator the main block of the analog part of the circuit. It causes the pulses to densify on the digital output signal. Compared to the input, the shape of the signal is different, but its nature is preserved [1], [2], [3].

Fig. 1 shows differential block scheme of $\Sigma - \Delta$ ADC. In this scheme, analog input signal is compared (by difference amplifiers) with reference signal coming from 1 - bit digital to analog converters (DACs). This modified signal is then integrated and compared to the reference voltage in comparators (in generally 0 V). Then looped to 1-bit DACs whose outputs are changing mentioned analog input reference in the difference amplifiers. D-type flip-flops are used for synchronization of digital output signal [4].

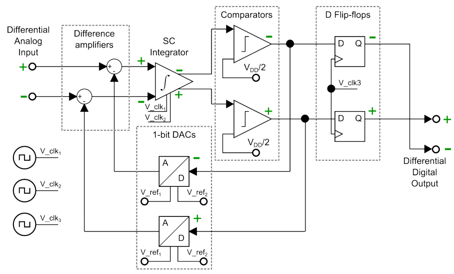

Fig. 1. The differential first-order signle-loop output-synchronized $\Sigma - \Delta$ ADC

In this paper, the principle of the integrator design is introduced in section II. The achieved results obtained from simulations are stated in section III and the evaluation of all process is summarized in the last section IV.

II. Proposed integrator

Topology of FD SC integrator block from Fig. 1 is introduced in the Fig. 2.

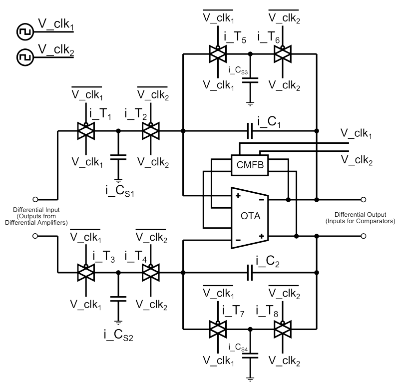

Fig. 2. Topology of FD SC integrator

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A. Operational transconductance amplifier - OTA

The topology of OTA is shown in the Fig. 3. This circuit is based on parallel connection of two-stage NMOS and PMOS OPAMPs working in sub-threshold regimes.

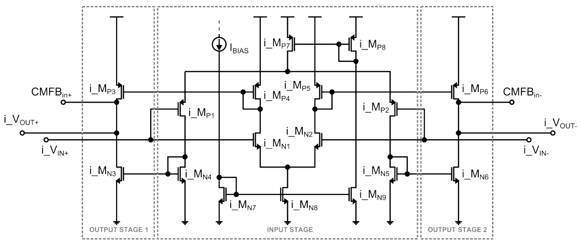

Fig. 3. Topology of OTA

Complementary connection of NMOS and PMOS in the OPAMP output stage allows RtR operation at output. It is well-know that input voltage range of PMOS transistor is limited from above by the voltage:

$$V_{PMOS_{MAX}} = V_{DD} - |V_{DS\_sat}(i\_M_{P7})| - |V_{TH}(i\_M_{P1})| \quad (1)$$

In the range from $V_{PMOS_{MAX}}$ to V_{DD} is NMOS transistor active only. Contrariwise, the input voltage range of NMOS transistor is limited from below by the voltage:

$$V_{NMOS_{MIN}} = V_{DS\_sat}(i\_M_{N8}) + V_{TH}(i\_M_{N1}) \quad (2)$$

In the range from ground to $V_{NMOS_{MIN}}$ is PMOS transistor active only.

Around the $\frac{V_{DD}}{2}$ voltage, both of transistors are in the active region. In the area where both amplifiers operate in the active region, the transconductances g_{m_NMOS} and g_{m_PMOS} are overlapped. In general, by increasing g_m, the dominant pole is shifted towards higher frequencies. This may result in frequency response and overall circuit stability. Transistors i_M_{N1}, i_M_{N2}, i_M_{P1} and i_M_{P2} have been designed with g_m compensation as is shown in Fig. 4:

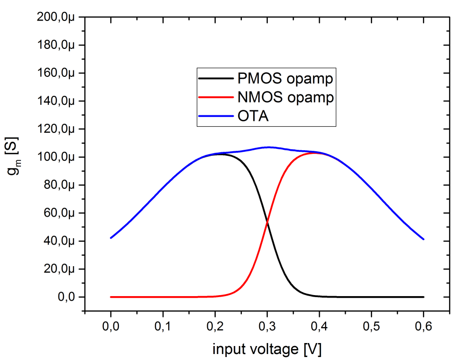

Fig. 4. Compensation of g_{m_PMOS} and g_{m_NMOS}

The input transistors (i_M_{N1}, i_M_{N2}, i_M_{P1}, i_M_{P2}) was set to the sub-treshold region by the equations:

$$V_{eff} = 2.V_T.n.\ln(\exp(\sqrt{IF}) - 1) \quad (3)$$

$$\frac{W}{L} = \frac{I_D}{I_{D0}.\exp(\frac{V_{eff}}{n.V_T})} \,. \quad (4)$$

The current sources (i_M_{P7}, i_M_{N8}) works in strong saturation by the V_{DS} voltage approximately 100 mV. Transistors i_M_{N7}, i_M_{N9} and i_M_{P8} was used as the simple current mirrors for circuit biasing. i_M_{P4}, i_M_{P5}, i_M_{N4} and i_M_{N5} was used as a current mirrors for output stage 1 and 2 [5].

As an output stage, AB class amplifier is used. Dimensions of the transistors i_M_{P3}, i_M_{N3}, i_M_{P6} and i_M_{N6} was designed for relatively high currents in that branches due to driving output capacitors and capacitors in CMFB circuit.

B. Clock-boost circuit

In order to control switching transistors in CMFB circuit clock-boost circuit was used. Its topology is shown in the Fig. 5. Two inverters at the beginning of the circuit modify the rising and the falling edges of the clock signal for better operate with. Cross-coupled NMOS transistors b_M_{N1} and b_M_{N2} together with the capacitors b_C_1 and b_C_2 are forming a charge pump. Pulses from the clock are shifted up by adding V_{DD} voltage to them. By the transistors b_M_{N3} and b_M_{N4} is this shifted voltage (in the other words: shifted charge) connected to a "bootstrap" capacitor b_C_3. By switching the transistors b_M_{P1}, b_M_{N5}, b_M_{P2}, b_M_{N6}, b_M_{N7}, b_M_{N8} and b_M_{N9} is mentioned charge transported to the output - switching transistor in SC CMFB circuit. This circuit was designed as a part of SC CMFB circuit as a "bootstrap" [2].

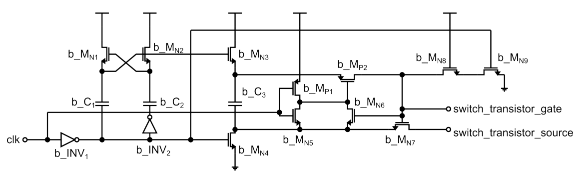

Fig. 5. Topology of clock-boost circuit

C. Switched-capacitor CMFB circuit

Fig. 6 shows the topology of the SC CMFB circuit. There are three task for CMFB circuit: sensing the common mode outputs i_V_{OUT+} and i_V_{OUT-} from fully differential OTA, comparison of the sensed results with a reference voltage V_{CM} (in this design, the reference voltage for CMFB circuit is equal to $\frac{V_{DD}}{2}$) and return the bias voltage V_{BIAS} back to the OTA by $CMFB$ output. This SC CMFB circuit is clocked by non-overlapping pulses with frequency $f_{sw} = 20\ MHz$. These pulses are shifted up in "bootstrap" circuits for better gate-switching of all the transistors in the Fig. 6 [2]. All the transistors have been designed with the same dimensions as a switches with a low enough R_{ON} parameter. The capacitors cm_C_1 (cm_C_2) and cm_C_3 (cm_C_4) have been designed with a specific ratio k:

$$k = \frac{cm\_C_1}{cm\_C_3} = \frac{cm\_C_2}{cm\_C_4} \tag{5}$$

In order to obtain low value of output offset, the specific ratio capacitors cm_C_1 (cm_C_2) and cm_C_3 (cm_C_4) should be perfectly set. However, cm_C_1 and cm_C_2 can not be too large, because OTA will not be able to drive them. On the contrary, cm_C_3 and cm_C_4 can not be too small, because the parasitic capacitance of the switching transistors will start to affect the circuit. Transistors cm_M_{P1}, cm_M_{P2}, cm_M_{N9} and cm_M_{N10} form the output invertors for driving the SC CMFB outputs. These outputs are connected to the OTA, as it is shown in the Fig. 2 and Fig. 3.

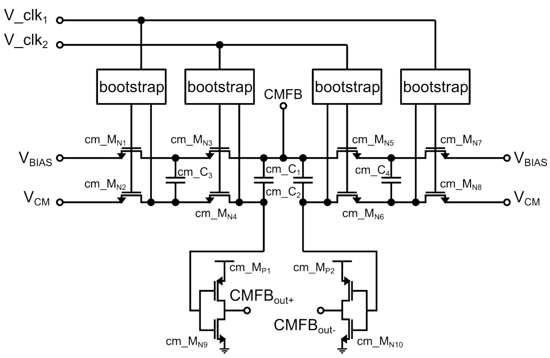

Fig. 6. Topology of switched-capacitor CMFB circuit

D. Switching transmission gates (T-gates)

As it is shown in the Fig 2., capacitors i_C_{S1} - i_C_{S4} are switched with transmission gates (T-gates) i_T_1 - i_T_8 for better charge transport. For initial values of capacitors, voltage gain and cutoff frequency the following equations can be used:

$$C_{sw} \propto \frac{1}{f_{sw}.R_{eq}} \tag{6}$$

$$A_{INT\_MAX} \propto \frac{i\_C_{S1}}{i\_C_{S3}} \tag{7}$$

$$f_{cutoff} = BW_{INT} \propto \frac{1}{2.\pi.i\_C_1.R_{eq}(i\_C_{S3})} \tag{8}$$

III. Achieved Results

The integrator has been simulated with the signals of varying frequencies, amplitudes and types. For DC simulation of the OTA (with disconnected SC CMFB circuit), the input voltage was swept in the range of GND and V_{DD}. In the AC simulation, two periodic sources with 180° phase shift were used for simulate differential input signal. Because of using clocks, periodic steady-state analysis (PSS analysis) and periodic AC analysis (PAC analysis) was used. In the Fig. 7 are shown the transfer responses of inverting and non-inverting outputs, where RtR output voltage range can be obtained. Fig. 8 shows frequency response of OTA with maximum gain of $A_{OTA\_MAX} = 46.16\ dB$. Bandwidth of proposed OTA is $BW_{OTA} = 24.23\ kHz$, while gain-bandwidth is $GBW = 5.03\ MHz$.

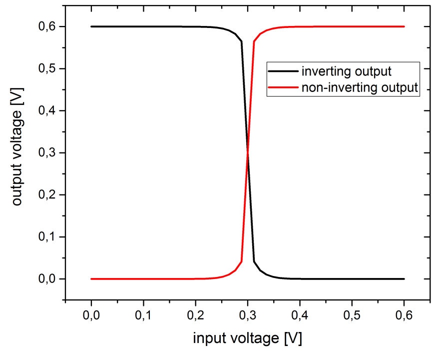

Fig. 7. Transfer response of OTA

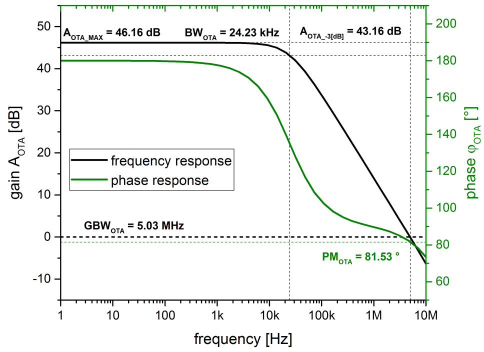

Fig. 8. Frequency and phase response of OTA

Fig. 9 shows frequency response of whole integrator where low-frequency gain of $A_{INT\_MAX} = 24.09\ dB$ and cutoff frequency $f_{cutoff} = 165.95\ kHz$ were achieved.

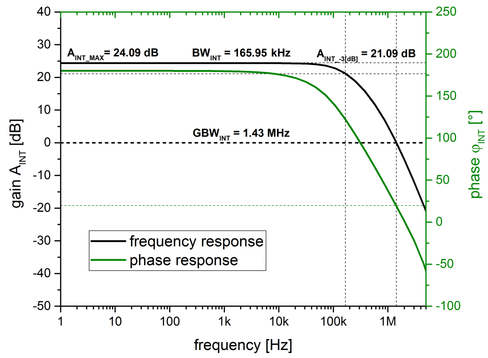

Fig. 9. Frequency and phase response of integrator

In Fig. 10 is shown time response of integrator to a harmonic input signal and Fig. 11 shows time response of integrator to a pulse input signal.

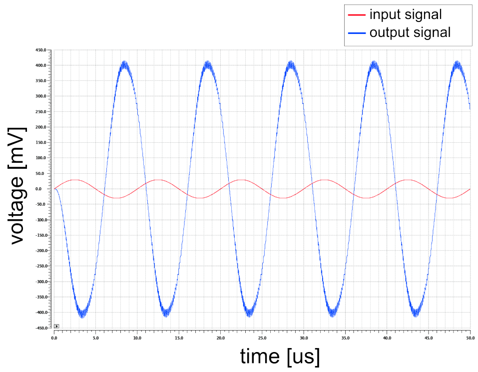

Fig. 10. Harmonic signal response - integration

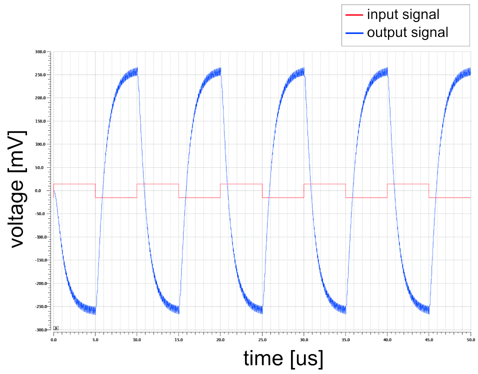

Fig. 11. Pulse signal response - integration

All the essential achieved parameters are summarized in the Tab. 1.

TABLE I. INTEGRATOR PARAMETERS

Parameter	Value
V_{DD}	$0.6\ V$
C_{LOAD}	$10\ pF$
A_{OTA_MAX}	$46.16\ dB$
BW_{OTA}	$24.23\ kHz$
GBW_{OTA}	$5.03\ MHz$
PM_{OTA}	$81.53°$
A_{INT_MAX}	$24.09\ dB$
BW_{INT}	$165.95\ kHz$
GBW_{INT}	$1.43\ MHz$
P_{INT}	$22.16\ \mu W$

In addition, interesting thing is the effect of the dimensions of transistor to shape of the switched signal. In the Fig. 12 is the signal switched by NMOS transistor of small dimensions.

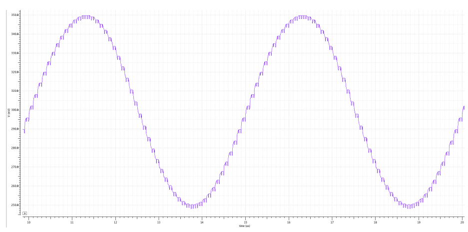

Fig. 12. Switched signal - W and L small enough

In the Fig. 13 is this signal switched by NMOS transistor with the same width as in the Fig. 12, but with increased length.

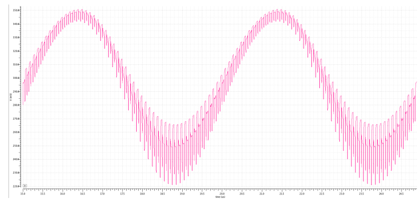

Fig. 13. Switched signal - small W, larger L

In the Fig. 14 is this signal switched by NMOS transistor with the same length as in the Fig. 12, but with increased width.

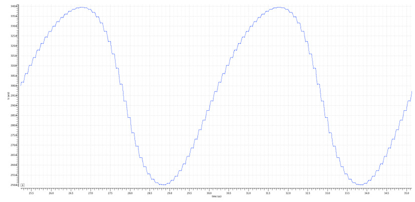

Fig. 14. Switched signal - small L, larger W

IV. CONCLUSION

Ultra low-voltage RtR fully differential switched-capacitor filter with supply voltage of 0.6 V was designed for load capacitance $10\ pF$. Power consumption of this circuit is $22.16\ \mu W$. If necessary, gain of the integrator $24.09\ dB$ can be increased by larger ratio of capacitors i_C_{S1} and i_C_{S3}. It is important to note, that for possibly increase the gain, it is necessary to design output stages of OTA for higher current values.

This switched-capacitor integrator will be used as the main part of currently designing Sigma-Delta analog to digital converter. Mentioned converter will be developed for energy-harvesting applications (solar panels, wind power stations etc.).

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