Series Capacitor Dual-output DC/DC Converter and Power Inverter with Reduced Switching Voltage and Stress on Switching Devices

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***Abstract*—This paper presents series capacitor dual inductor switching power convertor that features dual output capability and reduced $V_{DD}/2$ switching voltage. The dual output capability allows circuit to be configured as DC/DC power converter with two distinct outputs, or a DC/AC power inverter. The output voltage range is limited to $V_{DD}/2$, and it is therefore suitable for applications with high downscale ratio. The structure is based on a series capacitor topology which features reduced $V_{DD}/2$ switching voltage for both channels and also reduced $V_{DD}/2$ maximal ratings of switches and series capacitor. This reduces considerably the active area and dynamic (switching) power losses of the converter. Structure also feautures passive flying capacitor voltage balancing ensured by one reduced auxiliary capacitor.**

Keywords—three level power converter, dual output buck converter, series capacitor power converter.

I. Introduction

Multilevel power converters present a common way to reduce switching voltage and voltage stress on the switching devices. Reducing of the switching voltage has an important impact on the implementation cost as it allows to reduce inductor ripple current, and therefore size of passive LC output filter. Reduction of inductor size is advantageous not only for the cost and area aspects, but also allows to reduce ESR of the inductor and thus overal power dissipation.

Structures of multilevel power converters that features also reduce voltage rating of the switches allows simultaneously further decrease dynamic and ohmic power dissipation. However, this second aspect, together with gain of active area should be carefully evaluated, as typically more switching devices are connected in series. Moreover, switching voltage reduction is typically obtained by a flying capacitor presenting a non-negligible ESR and thus decreasing the power efficiency η.

Focus of this paper will be on the dual output power converter, that can also be configured as DC/AC power inverter. While dual output DC/DC converter target to generate two distinct DC output voltages, power inverter acts as an AC voltage generator, powered by an DC voltage source, such as photovoltaic (PV) panel.

Most frequently used multilevel-PWM power stages are listed *e.g.* in [1,2]. *Fig. 1*. Shows example of flying capacitors multilevel power stage. The flying capacitor power stage presents an efficient way to generate three or more level PWM signal. These power stages can also be used in a full H-bridge topology of a power inverter [3]. However, as mentioned in ref. [4], a precious capacitor balancing is required for correct device operation. The balancing of the flying capacitor requires complex feedback algorithm. This algorithm interacts with main PWM regulator of the output voltage by tiny adjustment of the duty-cycles of related switches, targeting to maintain accurate $V_{DD}/2$ voltage on C_{FLY}. As results, this

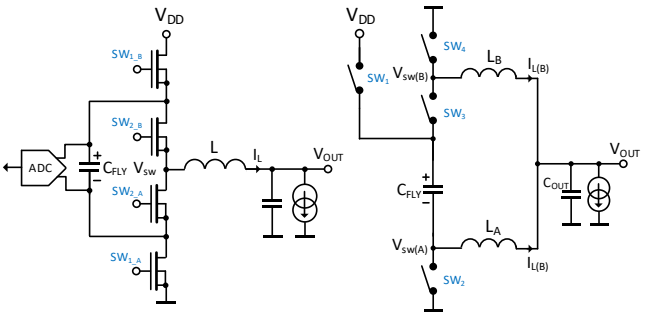

Fig. 1. a) structure of flying capacitor three-level power stage with voltage balancing circuit, b) series-capacitor dual-phase buck converter

structure is usually implemented only in three-level configuration [4].

Series capacitor buck converter [5] is very interesting way to provide automatic flying (or series) capacitor voltage balancing with reduced number of switches. It contains two switching nodes $V_{SW(A,B)}$, connected to individuals inductors. While outputs of LC filters are connected to a single output, any deviation of $V_{(CFLY)}$ from $V_{DD}/2$ is compensated by modulation of L_A and L_B inductor current. Due to reduced switching voltage toggling between 0 and $V_{DD}/2$, and also feature of complementary phases between switching nodes $V_{SW(A,B)}$, this circuit combine advantages of both multilevel and dual phase power converters. However, in contrast to complicated circuit solution shown in *Fig. 1 a*), voltage balancing of C_{FLY} is paid by one supplementary inductor.

Phase shifted carrier PWM power inverter shown in *Fig. 2* provides three-level PWM signal by generating asymmetrical duty-cycle for left and right half-bridges. Generated output voltage $V_{LX(OUT)} = V_{LX(L)} - V_{LX(R)}$ reaches three voltage levels: 0 and $\pm V_{DD}$. This technique offers previously mentioned

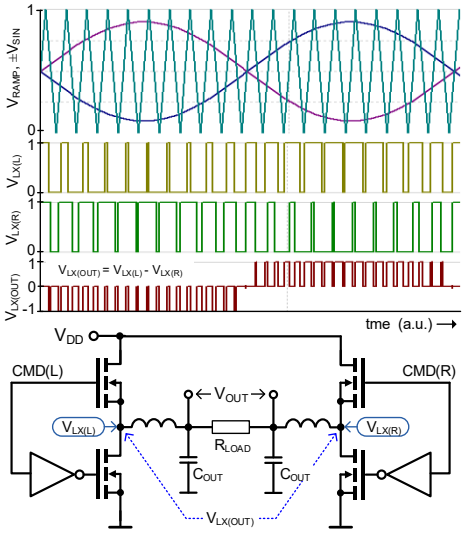

Fig. 2. Three-level shifted-carrier PWM H-bridge structure [2] with related control signals. $CMD_{(L,R)}$ are the control signals.

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advantage of inductor current and output voltage ripple reduction. However, transistors withstanding full drain-source voltage $V_{DSS} = V_{DD}$ are required.

Generally, dual output converters and theirs advanced control scheme are widely described in literature. Majority of the converter contains one inductor shared between two outputs [6], [7]. Beyond requirement of full-V_{DD} switches in these structures, sharing one inductor for two output channels increase a risk of the crosstalk. On this account, high-performance control algorithms are required.

Common issue of any hybrid topology that allows to reduce voltage of switches is that tradeoff between gain coming from reduced voltage (such as reduced channel length and thus R_{ON}, CV^2 power, or reduced LC filter size) is paid by increased complexity of the switching structure, including also feedback control scheme combining output voltage regulation, and flying capacitor voltage balancing. In this paper, dual output topology that reduces switch and capacitor voltages, and able to deliver output voltages up to $V_{DD}/2$ is described. It is based on hybrid series capacitor converter [5], combining flying (series) capacitor and inductors as energy storage elements. By dissociating outputs of both LC filters, an extra passive loop of C_{FLY} voltage balancing should be implemented. This passive loop contains two auxiliary switches and one capacitor C_{AUX}, and presents limited power dissipation and limited die area.

This article is organized as follows: in *2nd section*, main switching topology is described for the dual output buck converter and power inverter configurations. In *section III*, power dissipation aspects are discussed, while *section IV* present simulations in CMOS 0.35µm process.

II. Main Switching Structure

Switching structure for dual output DC/DC buck converter is depicted in *Fig. 3*, and for the power inverter providing DC-voltage to differential AC voltage conversion in *Fig. 4*. It is to be noted, that both structures can be used in reversed operation mode, *e.g. Fig. 3* as a dual-input boost converter, and *Fig. 4* as a synchronous rectifier/PFC circuit.

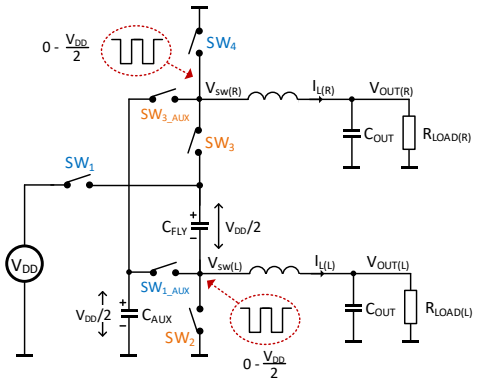

Fig 3. Switching structure for dual-output DC/DC converter.

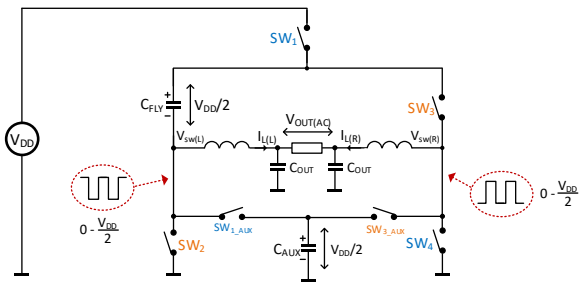

Fig 4. Switching structure for power inverter.

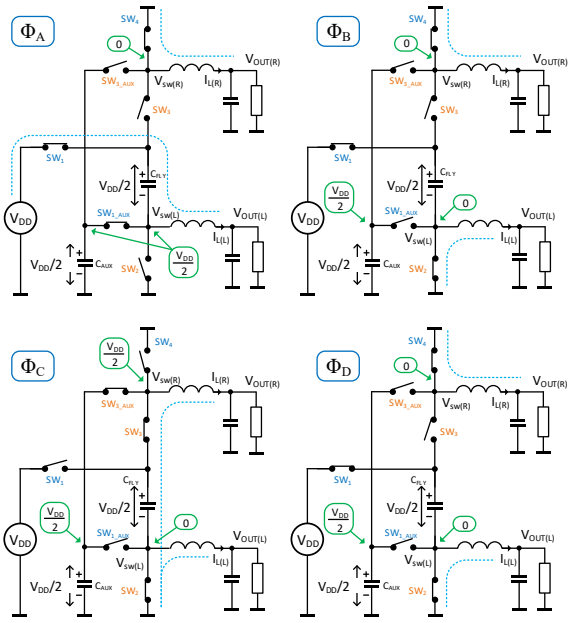

Fig 5. Switching phases for dual-output DC/DC converter from Fig. 3.

The switching phases of both circuits are identical, except that the output current in *Fig. 4* power inverter is not delivered against ground, but circulates between left and right outputs through load resistance R_{LOAD}. Detailed operations of both circuits can be described by switching phases $\Phi_{A,B,C,D}$.

A. Switching Phases of Dual-output DC/DC Converter

The operation of dual output converter from *Fig. 3* can be described by switching phases detailed in *Fig. 5*. Here, circuit operates in four switching phases $\Phi_{A,B,C,D}$. Phases B and C are identical, and can be therefore merged to improve the power efficiency. However, four phases description is provided here to demonstrate complete switching cycles of both switching nodes $V_{SW(L)}$ and $V_{SW(R)}$. Generally, order of phases can be altered and is provided here as an example.

Φ_A: during this phase, (+) plate of C_{FLY} is connected to V_{DD} by SW_1. Provided that voltage of C_{FLY} is $V_{DD}/2$, low-side switching node $V_{SW(L)}$ is set to $V_{DD}/2$. Voltage $V_{SW(L)}$ is also connected to auxiliary capacitor C_{AUX} *via* SW_{1_AUX}. Simultaneously, high-side switching node $V_{SW(R)}$ is connected to GND *via* SW_4. During this phase, C_{FLY} is charged by the coil current I_L and its voltage (charge) is therefore increasing (considering positive output current of $V_{OUT(L)}$ node). As we can notice from *Fig. 5*, both C_{FLY} and C_{AUX}, and also open switches SW_2, SW_{3_AUX} are biased by limited voltage $V_{DD}/2$. Switch SW_3, however is the sole open switch in the circuit exhibiting full V_{DD} voltage in the off-state.

$\Phi_{B,D}$: is producing zero switching-node voltages $V_{SW(L)}$ and $V_{SW(H)}$. C_{FLY} and C_{AUX} are kept floating, and all open switches are biased by reduced $V_{DD}/2$ voltage.

Φ_C: produces zero voltage $V_{SW(L)}$. (-) plate of C_{FLY} is then connected then to GND, and (+) plate is connected to $V_{SW(R)}$. As result, C_{FLY} set $V_{SW(R)}$ to $V_{DD}/2$. This signify, that C_{FLY} is now discharged by $I_{L(H)}$ and its voltage is decreasing (considering positive output current at $V_{OUT(R)}$ node). SW_{3_AUX} connect $V_{SW(R)}$ to auxiliary capacitor C_{AUX}, what allows to compensate any deviation of C_{FLY} voltage from target $V_{DD}/2$. All switches and capacitors are biased by limited $V_{DD}/2$ voltage.

The time duration of Φ_A and Φ_C, as well as average currents $I_{L(L)}$, $I_{L(R)}$ are generally not equals. Average charging and discharging currents of C_{FLY} during Φ_A and Φ_C could be therefore also not equals. Bias voltage of C_{FLY} can therefore significantly derive from target value $V_{DD}/2$. On this account, auxiliary capacitor C_{AUX} is ensuring charge transfer between $V_{SW(L)}$ and $V_{SW(H)}$ switching nodes during phases of Φ_A and Φ_C. This provide both switching voltages to be closely equals to desired value $V_{DD}/2$. Depending on the difference of output powers $P_{OUT(L)}$ and $P_{OUT(R)}$, C_{AUX} and associated switches are driving more or less important current. This effect is discussed in next section.

B. *Switching Phases of the Power Inverter*

Structure of the power inverter is identical to the dual output power converter described in the previous section. Only difference is that the load is connected between both outputs, and in PWM(t) modulation scheme allowing to generate complementary AC (*e.g.* sinewave) voltages.

Similarly, as described in previous section, phases Φ_A and Φ_C are providing $V_{SW(L)} = V_{DD}/2$, $V_{SW(R)} = 0$, and $V_{SW(L)} = 0$, $V_{SW(R)} = V_{DD}/2$, respectively. Likewise, capacitor C_{AUX} is used to compensate voltage difference between $V_{SW(L)}$ and $V_{SW(R)}$ during phases Φ_A and Φ_C. However, this difference is not originating from the difference of the output power delivered to the load as in *Fig. 3* circuit, but from the sum of power delivered by outputs $V_{OUT(L,R)}$. This aspect is a penalty of the converter in power inverter configuration *Fig. 4*, and will be discussed in next section.

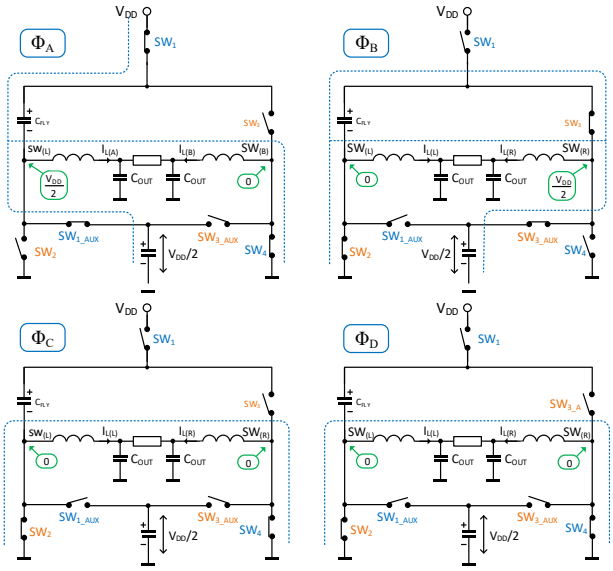

Fig. 6. Switching phases of DC/AC power inverter from Fig. 4.

III. Power Dissipation and C_{FLY} Voltage Balancing

As already mentioned, presented circuits rely on accurately regulated flying capacitor voltage. Any important deviation from target value $V_{DD}/2$ (with exception of steady ripple voltage) can misbalance the circuit, and also increase voltage stress on the switches. In standard flying capacitor multilevel power stages [3] shown in *Fig. 1 a)*, balancing of C_{FLY} is ensured by a complementary feedback loop requiring dedicated sensing of the flying capacitor voltage. Circuits presented in this paper are based on the passive balancing by virtue of C_{AUX}, compensating for charge difference delivered to inductors between phases Φ_A and Φ_C. In order to provide attractive performances of the circuit, this charge difference should be low. This allows to reduce value of C_{AUX}, and reduce area and power dissipation of SW_{1_AUX} and SW_{3_AUX}.

It will be shown in following, that the reduction of the charge difference delivered to inductors during phases Φ_A and Φ_C can be achieved by reducing difference between powers delivered by outputs $V_{OUT(L)}$, and $V_{OUT(R)}$. Obviously, this requirement limits the application scale of presented circuits to constant load scenarios, as for instance LED drivers.

Considering an idealized case where C_{FLY} is permanently charged to $V_{DD}/2$ (or replaced by $V_{DD}/2$ voltage source), average currents $\langle i_{CFLY(L,R)} \rangle$ referred to the powers delivered to $V_{OUT(L)}$, and $V_{OUT(R)}$ can be written as:

$$\begin{aligned} \left\langle i_{CFLY(L)} \right\rangle &= \frac{V_{OUT(L)}}{R_{LOAD(L)}} \cdot D_L \\ \left\langle i_{CFLY(R)} \right\rangle &= \frac{V_{OUT(R)}}{R_{LOAD(R)}} \cdot D_R \end{aligned} \tag{1}$$

where $D_{(L,R)}$ are the duty cycle ratios of switching nodes $V_{SW(R)}$ and $V_{SW(L)}$: $D_{(L,R)} \approx 2V_{OUT(L,R)}(t)/V_{DD}$. Previous equations can be rearranged as functions of output powers $P_{OUT(L,R)}$:

$$\begin{aligned} \left\langle i_{CFLY(L)} \right\rangle &= \frac{2}{V_{DD}} \frac{V_{OUT(L)}^2}{R_{LOAD(L)}} = \frac{2}{V_{DD}} P_{OUT(L)} \\ \left\langle i_{CFLY(R)} \right\rangle &= \frac{2}{V_{DD}} \frac{V_{OUT(R)}^2}{R_{LOAD(R)}} = \frac{2}{V_{DD}} P_{OUT(R)} \end{aligned} \tag{2}$$

In real circuit, average current $\langle i_{CFLY} \rangle$ of capacitor C_{FLY} in steady state should be zero. The difference between $\langle i_{CFLY(L)} \rangle$ and $\langle i_{CFLY(R)} \rangle$ should be therefore compensated by an external circuit realized by C_{AUX}. Optimization of the auxiliary branch relies in minimizing its active area and power dissipation. Average current driven by auxiliary switches can be expressed as $\langle i_{SW\_AUX} \rangle = \left(\langle i_{CFLY(L)} \rangle - \langle i_{CFLY(R)} \rangle \right)/2$, where term 2 appears due to the fact, that each switch conducts only half of the current compensating for the charge difference. The average current i_{SW_AUX} can be then expressed as:

$$\left| \left\langle i_{SW\_AUX} \right\rangle \right| = \frac{\left| P_{OUT(L)} - P_{OUT(R)} \right|}{V_{DD}} \tag{3}$$

As already mentioned, reduction of difference $P_{OUT(L)} - P_{OUT(R)}$ allows to decrease sizes and power dissipation of auxiliary switches and auxiliary capacitor C_{AUX}. It is to be noted, that the power dissipation of auxiliary switches and ESR of C_{AUX} are not given by average current (3), but by its RMS value. As $i_{SW\_AUX}(t)$ originates from the charge transfer between C_{FLY} and C_{AUX}, via switches resistances, it is governed by exponential function with time constant $R_{SW\_AUX} \cdot C_{AUX}$. Considering $C_{FLY} > C_{AUX}$, $i_{SW\_AUX}(t)$ can be written as:

$$i_{SW\_AUX}(t) \cong \frac{V_{CAUX(0)} - V_{SW(0)}}{R_{SW\_AUX}} \cdot e^{\frac{-t}{R_{SW\_AUX} C_{AUX}}} \tag{4}$$

Where $V_{CAUX(0)} - V_{SW(0)}$ is the initial difference between relevant switching node and V_{CAUX}. Equivalent power dissipation $P_{SW\_AUX} = R_{SW\_AUX} I_{SW\_AUX}^2$ can be obtained from definition of RMS current, by integrating squared exponential function (4) until T_{AUX_ON} (conduction time of the auxiliary switch) and averaging during $1/T_{SW}$:

$$P_{SW\_AUX} = \frac{C_{AUX}}{2T_{SW}} \left(e^{\frac{-T_{AUX\_ON}}{R_{SW\_AUX} C_{AUX}}} - 1 \right) \left(V_{CAUX(0)} - V_{SW(0)} \right)^2 \tag{5}$$

TABLE 1: POWER DISSIPATION IN TEST STRUCTURE FIG. 3. CORRESPONDING TO IDEAL CIRCUIT WITH ACCURATE TIMING. SIMULATION CONDITION WAS: V_{IN} = 10V, $V_{OUT(L)}$ = 1.2V, $V_{OUT(H)}$ = 0.93V, F_{SW} = 10MHz, D_L = 0.25, D_H = 0.2, C_{AUX} = 22nF, C_{FLY} = 68nF, $L_{R,L}$ = 1µH, R_{SW} = 50mΩ, R_{SWAUX} = 0.5Ω, $R_{LOAD(L)}$ = 2Ω, $R_{LOAD(R)}$ = 1Ω, P_{IN} = 1.66W, $P_{OUT(L)}$ = 0.732W, $P_{OUT(R)}$ = 0.87W.

switch	$I_{(AVG)}$ [mA]	$I_{(RMS)}$ [mA]	RI^2 [mW]
SW_1	166.6	341.3	5.82
SW_{1_AUX}	15.3	91.3	**4.17**
SW_2	621.4	788.3	31.1
SW_3	167.9	376.7	7.1
SW_{3_AUX}	18.6	56.3	**1.58**
SW_4	746.0	836.0	34.9
C_{FLY}	0	508.3	ESR = 0
C_{AUX}	0	107.2	ESR = 0
Σ power loss:		**84.7mW**	

It can be shown, that during the charging of capacitor C_{AUX}, half of the energy $C_{AUX}\Delta V^2$ required from the source to increase capacitor voltage by ΔV is dissipated on the switch resistance, and second half ($\frac{1}{2}C_{AUX}\Delta V^2$) remains accumulated in capacitor. On this account, power dissipation on R_{SW_AUX} is independent on R_{SW_AUX} and is equal to $\frac{1}{2}F_{SW}C_{AUX}\Delta V^2$. Beyond reduction of power difference (3), and initial voltage difference ΔV (determined by C_{FLY} and C_{AUX}), minimization of switch area can be obtained through increasing R_{ON_AUX}. This resistance should be chosen so, that the charge transfer is completed right at the end of T_{AUX_ON}. As consequence, peak of $i_{SW\_AUX}(t)$ can be reduced. This is advantageous to improve EMI and reliability parameters of semiconductor switches.

In the case of the power inverter, the cycle average values of $\langle i_{SW_{AUX}}(t)\rangle$ vary with phase (t) of generated sinewave. As both outputs are sharing one load resistance, average current in left and right inductors are equals. Moreover, while positive current is generated by the branch with higher voltage, second branch absorbing the current is delivering negative current. Unfortunately, this increases the charge delivered by C_{AUX}. While $I_{COIL(R,L)}$ is now equal to $\pm V_{OUT}(t)/R_{LOAD}$, averaged current "requested" from C_{FLY} during phases Φ_A and Φ_C can be written as:

$$\left\langle i_{CFLY(R,L)}(t)\right\rangle = \pm\frac{V_{OUT}(t)}{R_{LOAD}}\cdot D_{(R,L)}(t) \qquad (6)$$

where $D_{(R,L)}$ are duty cycles of switching nodes $V_{SW(L,R)}$: $D_{(L,R)} \approx 2V_{OUT(L,R)}(t)/V_{DD}$. $\langle i_{CFLY(R,L)}\rangle$ can be then written as:

$$\left\langle i_{CFLY(R,L)}(t)\right\rangle = \pm\frac{V_{OUT}(t)}{R_{LOAD}}\frac{2V_{OUT(L,R)}(t)}{V_{DD}} \qquad (7)$$

As C_{FLY} average current in steady state should be zero, difference between $\langle i_{CFLY(R,L)}\rangle$ should be compensated by C_{AUX}. Auxiliary switches then drive sum of currents $\langle i_{CFLY(L)}\rangle + \langle i_{CFLY(R)}\rangle$ (7):

$$\left|\left\langle i_{SW\_AUX(t)}\right\rangle\right| = \frac{V_{OUT}(t)}{R_{LOAD}V_{DD}}\left|V_{OUT(R)}(t)+V_{OUT(L)}(t)\right| \qquad (8)$$

It results, that i_{SW_AUX} can be reduced by operation with low value of common-mode voltage $(V_{OUT(R)} + V_{OUT(L)})/2$.

IV. SIMULATION RESULTS

Performances of presented converter were verified by simulation of 10MHz circuit built with ideal and 0.35µm CMOS switches. The switching phases were kept separate as described in previous section. However, it is preferable to merge phases $\Phi_{B,D}$ to reduce switching power. *Tab. 1* provides summary of the power dissipation contributors generated with ideal simulation circuit (ideal resistance, capacitors, and no non-overlapping). Here, we can see RMS and average currents, and corresponding dissipated power RI^2. It can be seen that auxiliary switches dissipate ≈ 5.5mW. This corresponds to 0.3% of power efficiency loss.

Example of captured waveforms from SPICE simulation in 0.35µm process are shown in *Fig. 7*. This figure contains both switching nodes, output voltages, and inductor currents. The switching voltages contains ~2ns non-overlapping times. Comparted to previous simulation, SPICE simulation also contains extra switching power losses, due to commutation of gate voltages and mentioned non-overlapping intervals.

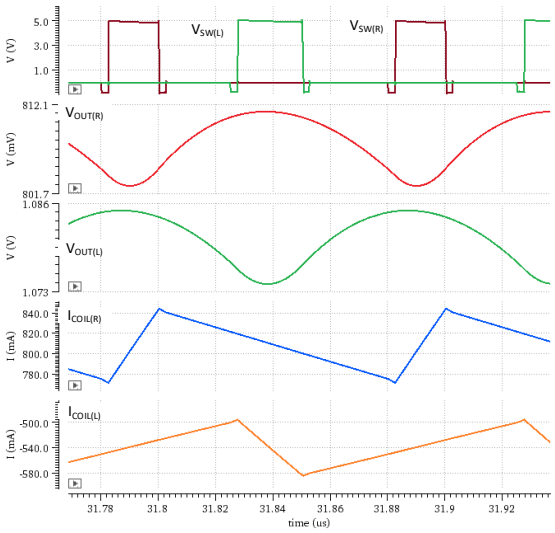

Fig. 7. Simulation example of the Fig. 3 circuit in 0.35µm CMOS process with BSIM3 models, and with parameters mentioned in Tab. 1 caption.

CONCLUSON

Presented paper presents series capacitor DC/DC converters with dissociated outputs. The voltage balancing of the series capacitor is ensured by passive charge transfer loop realized by auxiliary capacitor. It was shown, that for similar output power, additional voltage balancing loop exhibits negligible power dissipation, and can be designed with reduced area switches. Simulation demonstration with BSIM3 models in 0.35µm CMOS was also provided.

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