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Design of cooling system of power-electronics

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1. Introduction

The increasing pressure to produce electro and hybrid vehicles requires effective handling of power electronics. In the inverter, there is a printed circuit board (PCB) with chips belonging to power electronic kind. It means their power losses are in tens of watts each. These chips are MOSFETs or IGBTs (type of chip depends on specific hybrid application) usually. The produced heat causes thermal damage to the chips over lifetime and induces destruction of the whole inverter. Thus, it is necessary to design a cooling system for these chips very carefully.

Decreasing temperature is not the only objective the designer of the component needs to face in. Generally, there is also a requirement to have low pressure loss of the coolant medium as possible. It influences the efficiency of the complete system including pumps for circulation. However, these two demands are in contradiction against each other.

The last demand is to balance temperature in a chip row to avoid unwanted thermoelectric effects e.g., the Seebeck one [1].

2. Geometry model

The inverter model is for the calculation simplified to area around chips which need to be cooled by water-glycol mixture to reduce their temperature. The main parts of the model are inlet and outlet piping, housing, cooler body with pins pattern and chips. These parts are given. Due to some freedom in design, there is possible to modify pins pattern to match the above-mentioned demands.

The channel system is optimized to produce the maximal cooling performance with the lowest pressure loss respecting manufacturing restrictions, see Fig. 1.

3. Used software and simulation model

For the calculation FloEFD computation software (from Siemens) was used. Its big advantage is that it can be embedded to a CAD (Computer Aided Design) software – in this case to Creo Parametric. FloEFD uses an automatic cartesian mesh without any need to manually create invers geometry for area of fluid. It has three kinds of cell – solid, solid/fluid, and fluid. In the solid/fluid cells there is boundary layer based on the Prandtl boundary layer equations for a coarse mesh or Van Driest [2] approach for a fine mesh, [3].

The approach of FloEFD to creating a mesh is very fast and do not require time-consuming pre-processing of the geometry itself.

The important part of the simulation model is setting the simplified chip properties as a two-resistor component. It requires to define power-loss of the chip module and thermal resistance acquired from manufactures datasheet or measurement. In another words, chips produce heat

based on the power-loss and their thermal characteristic is described by thermal resistance, which is dependent on geometry and material properties as well as a manufacturing quality.

The simulation focuses on steady state. It produces the worst-case scenario of reaching maximum chip temperature and reduce calculation time.

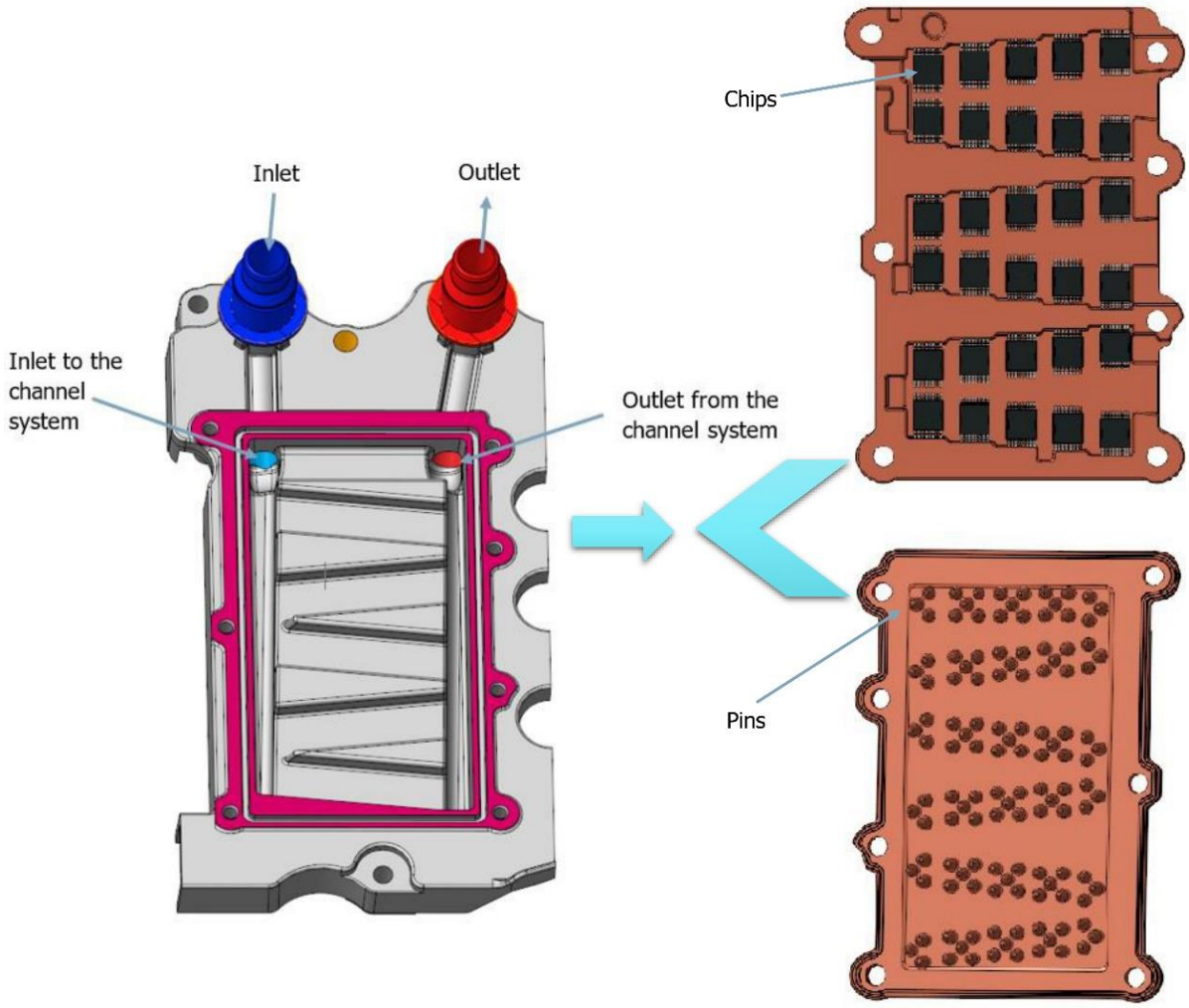

Fig. 1. Initial geometry of the model

4. Results

To obtain results for this contribution, 4 variants of the pins pattern were calculated. One with the original geometry and three improved versions of the pins pattern, see Fig 2.

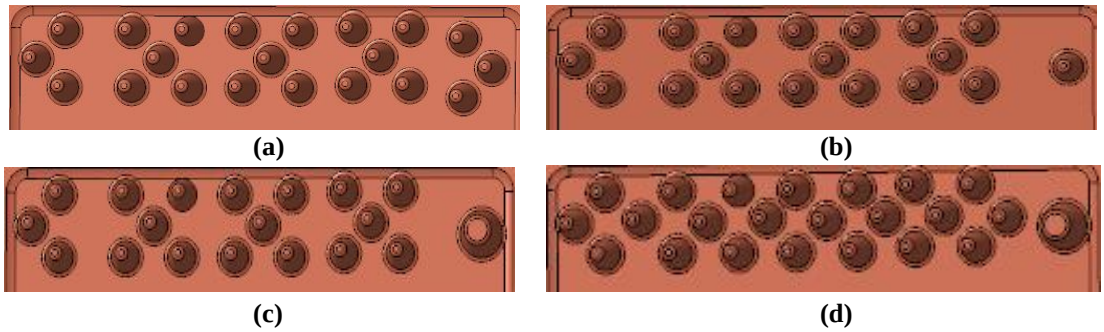

Fig. 2. Pins optimalization: (a) corresponds to initial geometry and thus Design 1, (b) it is Design 2, (c) corresponds to Design 3 and (d) to Design 4

In each geometrical variant 4 load cases (LCs) were set. There are distinguished by amount of the coolant entering to the system per minute and its temperature. The coolant temperature is identical to the ambient one. These load cases are as follows: 5 l/min @ 75°C (LC1), 10 l/min @ 75°C (LC2), 5 l/min @ 25°C (LC3) and 2 l/min @ -25°C (LC4).

The main observed effects of geometry changes are shown in Fig. 3. There is visible a percentual change in comparison to the original geometry. The higher percentage number at temperature means lower temperature and higher percentage number at pressure loss stands for lower pressure loss. It measures the benefits of the improvement.

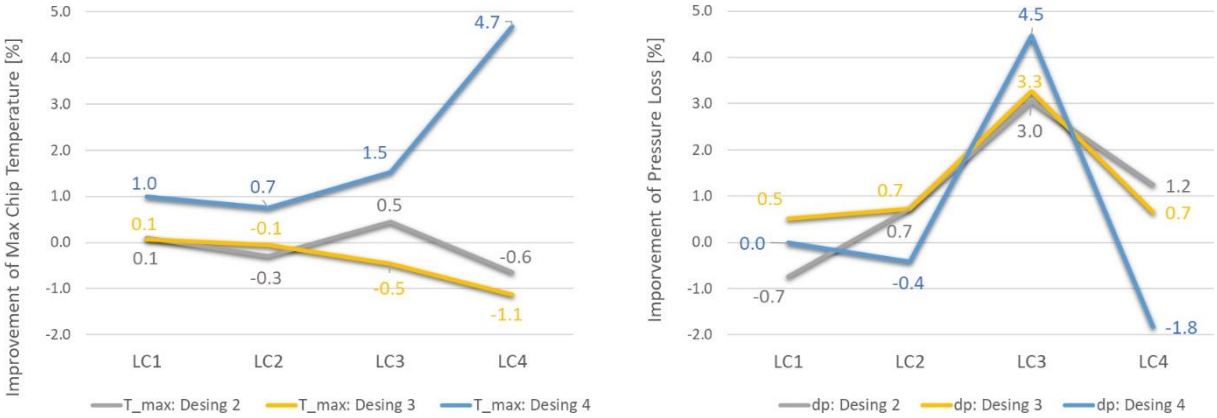

Fig. 3. Improvement of max chip temperature and pressure loss in %

5. Conclusion

Totally, 16 calculations were done. There were 4 geometrical variants and 4 load case scenarios for each geometry. The most feasible results are from the Design 4, where the first pin in a row is bigger than others and the pins are not only under the chips In this design the improvement of maximal chip temperature is up to 4.7 % depending on the load case. The negative impact on the pressure loss is still reasonable. However, the improvements of maximal chip temperature can look small it significantly decreases the risk of failure and increase the inverter lifetime and reliability.

References

[1] Kumar, A., et al., A review on fundamentals, design and optimization to high ZT of thermoelectric materials for application to thermoelectric technology, Journal of Electronic Materials 50 (2021) 6037-6059.

[2] Van Driest, E.R., On turbulent flow near a wall, Journal of Aeronautic Sciences 23 (11) (1956) 1007-1011.

[3] Simcenter FLOEFD™ for Creo® Technical Reference, Software version 2021.1, 2021.